January 1990
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FUJITSU

DATA SHEET

MB81461-12/-15

262,144-BIT DUAL PORT DYNAMIC RANDOM ACCESS MEMORY

262,144 Bit Dual Port DRAM

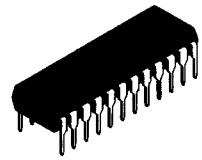
The Fujitsu MB81461 is a fully decoded, dynamic NMOS random access memory organized as 65,536 words by 4 bits dynamic RAM port and 256 words by 4 bits serial access memory (SAM) port.

The DRAM port is identical to the Fujitsu MB81464 with four bits of parallel random access I/O while the SAM port is designed as four 256-bit registers, each operating as a serial I/O. The four serial registers operate in parallel with each other during SAM port operation. Internal interconnects give the device the capability to transfer data bi-directionally between the DRAM memory array and the SAM data registers.

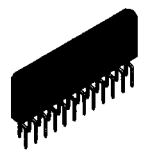
The MB81461 offers complementary asynchronous access of both the DRAM and SAM ports, except when data is transferred between them internally. The design is optimized for high speed and performance making the MB81461 the most efficient solution for implementing the frame buffer of a bit-mapped video display system. Multiplexed row and column address inputs permit the MB81461 to be housed in a 400-mil wide 24-pin DIP or ZIP package. Pinouts conform to the JEDEC-approved pinouts.

The MB81461 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process technology. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimum chip size. All inputs and outputs are TTL compatible.

- Dual Port Organization
  64 K x 4 Dynamic RAM port (DRAM)
  256 x 4 Serial Access Memory port (SAM)
- 24-pin DIP and ZIP packages
- Silicon-gate, Triple Poly NMOS, single transistor cell
- DRAM Port
  Access Time (t_{RAC})
  120 ns max. (MB 81461-12)
  150 ns max. (MB 81461-15)
  Cycle Time (t_{SAC})
  230 ns max. (MB 81461-12)
  260 ns max. (MB 81461-15)
- SAM Port
  Access Time (t_{SAC})
  40 ns max. (MB 81461-12)
  60 ns max. (MB 81461-15)
  Cycle Time (t_{SC})
  40 ns max. (MB 81461-12)
  60 ns max. (MB 81461-15)
- Single +5 V Supply, ±10% tolerance
- Real Time, Read Transfer capability
- Page Mode capability
- Power Dissipation
  DRAM; Act/SAM; Stby
  523 mW max. (MB 81461-12)
  468 mW max. (MB 81461-15)
  DRAM; Stby/SAM; Act
  275 mW max. (MB 81461-12)
  220 mW max. (MB 81461-15)
  DRAM; Stby/SAM; Stby
  110 mW max.
- Bi-directional data transfer between DRAM and SAM
- Fast serial access asynchronous to DRAM except transfer operation
- Bit Masked Write Mode capabiltiy
- 256 refresh cycles every 4 ms
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, Hidden Refresh capability
- Delayed write and Read-Modify-Write capability
- Standard 24-Pin Plastic Packages:
  DIP (MB81461-XXP)
  ZIP (MB81461-XXPSZ)

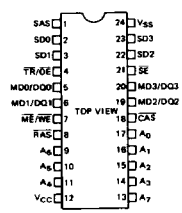


PLASTIC PACKAGE
DIP-24P-M04



PLASTIC PACKAGE
ZIP-24P-M02

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Storage Temperature	T_{STG}	-55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	—	50	mA

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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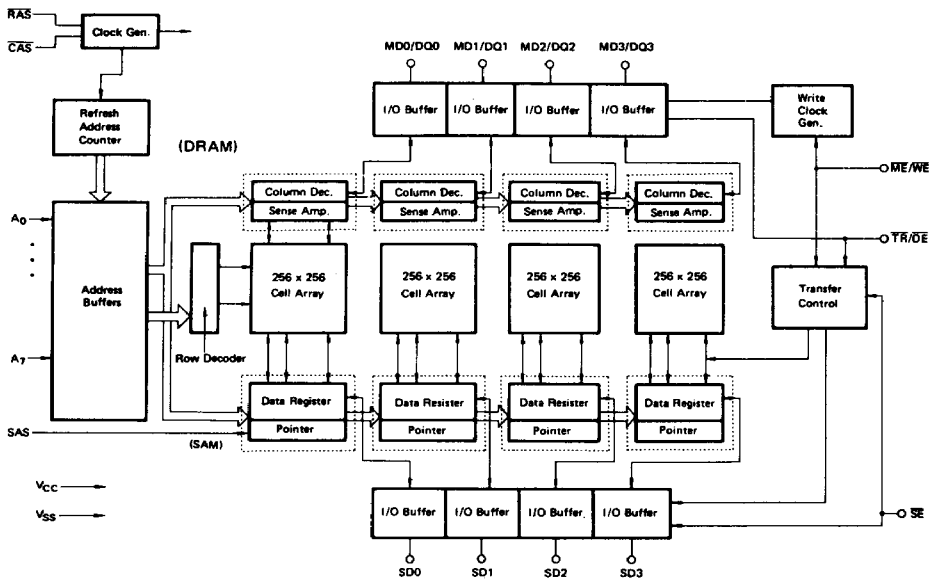
Fig. 1 – BLOCK DIAGRAM OF MB 81461 and PIN DESCRIPTION

Block Diagram



Pin Description

Pin Number		Symbol	Parameter	Mode
DIP	ZIP			
1	7	SAS	Serial Access Memory Strobe	Input
2,3,22,23	8,9,4,5	SD0 to SD3	Serial Data I/O	I/O
4	10	$\overline{TR}/\overline{OE}$	Transfer Enable/ Output Enable	Input
5,6,19,20	11,12,1,2	MD0/DQ0 to MD3/DQ3	Mask Data/Data I/O	I/O
7	13	$\overline{ME}/\overline{WE}$	Mask Mode Enable/Write Enable	Input
8	14	$\overline{RAS}$	Row Address Strobe	Input
17, 16, 15 14, 11, 10 9, 13	23,22,21, 20,17,16, 15,19	A_0 to A_7	Address Input	Input
12	18	V_{CC}	Supply Voltage +5 V	Power Supply
18	24	$\overline{CAS}$	Column Address Strobe	Input
21	3	$\overline{SE}$	Serial port Enable	Input
24	6	V_{SS}	Ground	Power Supply

DESCRIPTION

DRAM OPERATION

$\overline{RAS}$;

This pin is used to strobe eight row-address inputs from A0 to A7 pins and is used to select the operation mode of subsequent cycle, such as DRAM operation or transfer operation (by $\overline{TR}/\overline{OE}$ and bit mask write cycle or not (by $\overline{ME}/\overline{WE}$ and MD0/DQ0 to MD3/DQ3). Since $\overline{RAS}$ = "L" is the active condition of circuit, to maintain $\overline{RAS}$ = "H" (standby condition) is effective to save power dissipation.

$\overline{CAS}$;

This pin is used to strobe eight column address inputs at the falling edge. $\overline{CAS}$ pin has the function to enable and disable the output at "L" and "H" respectively during the read operation.
Another function of $\overline{CAS}$ is to select "early write" mode conditioned by $\overline{ME}/\overline{WE}$ = "L".

$\overline{ME}/\overline{WE}$;

This pin is used to select read or write cycle. $\overline{ME}/\overline{WE}$ = "L" select write mode and $\overline{ME}/\overline{WE}$ = "H" select read mode. This pin is also used to enable bit mask write cycle. If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write is enabled.

$\overline{TR}/\overline{OE}$;

This pin is used to select Transfer operation or not at the falling edge of $\overline{RAS}$, $\overline{TR}/\overline{OE}$ = "H" enables DRAM operation and $\overline{TR}/\overline{OE}$ = "L" enables Transfer operation between DRAM and SAM. After the falling of $\overline{RAS}$ with t_{YH}, this pin is used for output enable.
The $\overline{TR}/\overline{OE}$ controls the impedance of the output buffers. $\overline{TR}/\overline{OE}$ = "H" forces the output buffers at high impedance state. $\overline{TR}/\overline{OE}$ = "L" leads the output buffers at low impedance state. But in early write cycle, the output buffers are high impedance state even if $\overline{TR}/\overline{OE}$ is low.

A0 to A7;

These are multiplexed address input pins and used to select 4 bits of 262,144 memory cell locations in parallel within the MB 81461. The eight row address inputs are strobed by $\overline{RAS}$ and followed eight column address inputs are strobed by $\overline{CAS}$. These are used to select the start address of serial access memory also.

MD0/DQ0 to MD3/DQ3

These are common I/O pins of DRAM port. I/O mode is as specified for each function mode in the truth table.

Data Outputs:

The output buffers have three-state capability "H", "L" and "High-Z". To get valid output data on the pins, one of the read operations is selected such as "read" or "read-modify-write" mode. During a refresh cycle, either $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ mode is selected, output buffers are set in "High-Z" state.

Data inputs:

These are used as data input pins when a data write mode such as "Early-Write", "Delayed Write" or "Read-modify-Write" is selected. In any of the above cases, these pins are set at "High-Z" state to enable data-in without any bus conflict.
In any operation mode, read, write, refresh, transfer and their combined functions, output states "H", "L", "High-Z" are set by control signals $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$ and/or $\overline{TR}/\overline{OE}$. When "Bit mask write" mode is set, these pins are used as a control signal for write inhibit with MDi/DQi = "L" on the selected bit i.

Page Mode;

The page mode operation is to strobe the column address by $\overline{CAS}$ while $\overline{RAS}$ is maintained at "L" through all the successive memory operations if the row address doesn't change. This mode can save power dissipation and get the faster access time due to the elimination of $\overline{RAS}$ falling edge function.

Refresh;

Refresh of the DRAM cells is performed for every 256 rows per every 4 milliseconds.
The MB 81461 offers the following three types of refresh.

1) $\overline{RAS}$-Only refresh; The $\overline{RAS}$-Only refresh is performed with $\overline{CAS}$="H" condition. Strobing every 256 row addresses with $\overline{RAS}$ will complete all bits of memory cell to be refreshed while all outputs are invalid due to "High-Z" state. Further $\overline{RAS}$-only refresh saves the power dissipation substantially.
2) $\overline{CAS}$-before-$\overline{RAS}$ refresh; The $\overline{CAS}$-before-$\overline{RAS}$ refresh offers an alternate refresh method. If $\overline{CAS}$ is set low for the specified period (t_{FCS}) before the falling edge of $\overline{RAS}$, refresh control clock generator and refresh address counter are enabled, and an refresh operation is performed. After the refresh operation is performed, the refresh address counter is incremented automatically for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3) Hidden refresh; The hidden refresh is performed by maintaining the valid data of last read cycle at MD/DQ pins while extending $\overline{CAS}$ low. The hidden refresh is equivalent to $\overline{CAS}$-before-$\overline{RAS}$ refresh because $\overline{CAS}$ stays low when $\overline{RAS}$ goes to low in the next cycle.

Bit Mask Write;

This mode is used when some of the bits should be inhibited to be written into cells. The bit mask write mode is executed by setting $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$ during write mode (early, delayed write or read-modify-write cycle). The bits to be masked (or inhibited to write) is determined by MD/DQ state at the falling edge of $\overline{RAS}$, for example, if MD0/DQ0 and $\overline{ME}/\overline{WE}$ are both low at the falling edge of $\overline{RAS}$, the data on MD0/DQ0 pin is not written into the cell during the cycle. Refer to the Fig. 2.

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EXAMPLE OF BIT MASK WRITE OPERATION

Falling edge of $\overline{RAS}$						Function
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{WE}$	MD0/DQ0	MD1/DQ1	MD2/DQ2	MD3/DQ3	
H	H	X	X	X	X	Write enable
	L	H	L	H	L	Write enable for DQ0 and DQ2 Write disable for DQ1 and DQ3

X: Don't Care

FUNCTIONAL TRUTH TABLE FOR DRAM OPERATION

$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$	$\overline{TR}/\overline{OE}$	ADDRESSES	MD0/DQ0 to MD3/DQ3	Function
H	H	X	X	X	X	Standby
L	L	H	H→L	Valid	Valid Data Out	Read
L	L	L*	H→X	Valid	Valid Data In	Early Write
L	L	H→L	H → X → H	Valid	Valid Data In	Delayed Write
L	L	H→L	H→L→H	Valid	Valid Data Out → Valid Data In	Read-Modify-Write
L	H	X	H→X	Row address	High-Z	$\overline{RAS}$-Only Refresh
H→L	L	X	H→X	X	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ Refresh

*: If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write mode is enabled.

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TRANSFER OPERATION:

The transfer operation is featured in the MB 81461B. This mode is used to transfer simultaneously 256x4 data from DRAM to SAM or from SAM to DRAM. The direction of transfer is determined by the state of $\overline{ME}/\overline{WE}$ at the falling edge of $\overline{RAS}$. $\overline{ME}/\overline{WE}$="H" defines the transfer from DRAM to SAM (Read Transfer Cycle) and $\overline{ME}/\overline{WE}$="L" defines the transfer from SAM to DRAM (Write Transfer Cycle).

I/O mode of SD0 to SD3 determined while the transfer operation is set ($\overline{TR}/\overline{OE}$="L") conjunctioned with $\overline{ME}/\overline{WE}$ state.

After Read Transfer Cycle, please apply two or more SAS Clock.

$\overline{TR}/\overline{OE}$;

This pin is used to enable transfer operation at the falling edge of $\overline{RAS}$.

$\overline{ME}/\overline{WE}$;

This pin is used to select the direction of transfer at the falling edge of $\overline{RAS}$.

A0 to A7;

These pins are used to select the row address of DRAM port to be transfered from or to, and the start address of SAM port for the serial read or write operation. The row address is strobed by $\overline{RAS}$ and the start address is strobed by $\overline{CAS}$.

Pseudo Write Transfer:

To start serial write cycle, the SD pins must be set in input mode. To do this, write transfer cycle should be executed. The pseudo write transfer cycle is to change the SD pins into input mode without data transfer from SAM to DRAM. Refer to Fig. 3.

Refresh during transfer cycle;

DRAM and SAM are refreshed during transfer cycle as shown below.

1) Read transfer cycle:
   During read transfer cycle, the selected row address of DRAM to be transfered to SAM is refreshed. SAM data are kept by applying 256 SAS clocks within 4 ms after the read transfer cycle.
2) Write transfer cycle:
   During write transfer cycle, the new data are written from SAM to DRAM and this row address should be refreshed within 4 ms.
   But SAM data are not refreshed during write transfer cycle. Therefore, the SAM refresh (applying 256 SAS clocks within 4 ms) must be executed. Especially, when the write transfer cycle is executed continuously, 256 SAS clock should be applied within 4 ms.

SERIAL ACCESS OPERATION:

The MB 81461 has 256 words by 4 bits Serial Acess Memory (SAM) corresponding to 64K words by 4 bits DRAM and the fast serial read/write access is achieved by SAM architecture. Read or write cycle is determined when the last read or write transfer operation is executed. If the last transfer operation was read transfer, the serial read cycle is performed until the next write or pseudo write transfer cycle is executed. On the other hand, if the last transfer operation was write or pseudo write or pseudo write transfer, the serial write cycle is performed. In the serial write operation, 256 words by 4 bits data stored in the SAM can be transfered to DRAM under $\overline{SE}$="L" condition, and $\overline{SE}$="H" condition disables data transfer from SAM to DRAM. The serial access operation can be done asynchronously from DRAM port.

SAS;

This pin is used as a shift clock for SAM port. The serial access is triggered by the rising edge of SAS. In the write cycle, the data of the SD pins are strobed by the rising edge of SAS and written into the selected cell. In the read cycle, out-

put data become valid after t_{SAC} from the rising edge of SAS and the data remain valid until the next cycle is defined. The SAS clock increments the SAM address automatically. When the SAM address exceeds #255 (Most Significant Address) it returnes to #0 (Least Significant Address).

$\overline{SE}$;
This pin is used to enable serial access operation by bit to bit. $\overline{SE}$ = "H" disables serial access operation. In the serial read operation, this pin is used for output enable, i.e., $\overline{SE}$ = "H" leads SD pins to "High-Z" state. $\overline{SE}$ = "L" leads SD pins to valid data with specified access time. In the serial write operation, this pin works as write enable control pin.

SD0 to SD3;
These are used as data input/output pins for SAM port. Input or output mode is determined by last occured transfer operation, if last transfer operation was read transfer mode, they are output mode. If the write transfer mode was set, SD pins are enabled to write data into SAM.

Refresh;
Since the SAM is constructed by dynamic circuitry, the refresh is necessary to maintain the data in it. The refresh of SAM must be done by 256 cycles of SAS clock/4ms in either output or input mode. $\overline{SE}$ = "H" allows refresh of SAM with SD pins at "High-Z" state.

Real Time Read Transfer;
This feature is applicable to obtain valid data continuously when row address is changed without any timing loss from the last bit of previous row to the first bit of new row. Data transfer from DRAM to SAM is triggered by rising edge of $\overline{TR}/\overline{OE}$ after the preparation of internal circuit for this operation, while SAM port can continue read operation asynchronously from the above mentioned internal move. Once $\overline{TR}/\overline{OE}$ returns to "H" with the restricted timing specification t_{TSL} and t_{TSD} refered to SAS clock, SD pins can get the valid output data continuously as shown in Fig. 4. The key issue to achieve this feature is to apply SAS clock continuously with the timing consideration to the rising edge of $\overline{TR}/\overline{OE}$.

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FUNCTIONAL TRUTH TABLE FOR SERIAL ACCESS (Asynchronous from DRAM port)

Falling edge of $\overline{RAS}$		SAS	$\overline{SE}$	SD0 to SD3	Function
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{WE}$				
H	X	Clock	L	Input/Output*	Sequential access enable
		Clock	H	Input/Output*	Sequential access disable

*: The read or write operation of SAM port is pre-determined by the last occurred transfer cycle. Input mode is for write operation. Output mode is for read operation.

X; Don't Care

Fig. 2 – EXAMPLE OF BIT MASK WRITE OPERATION

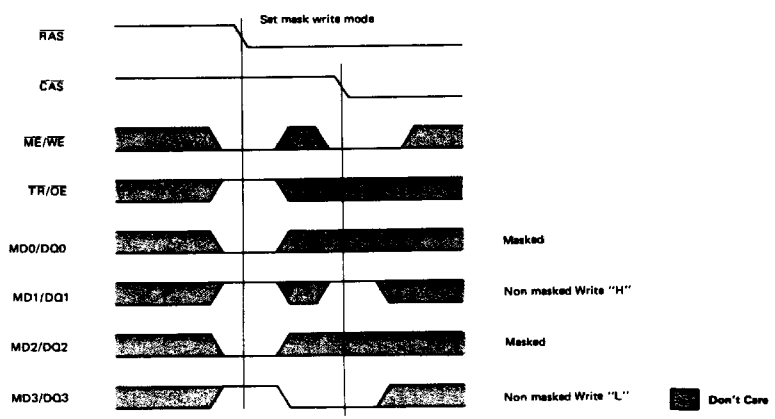

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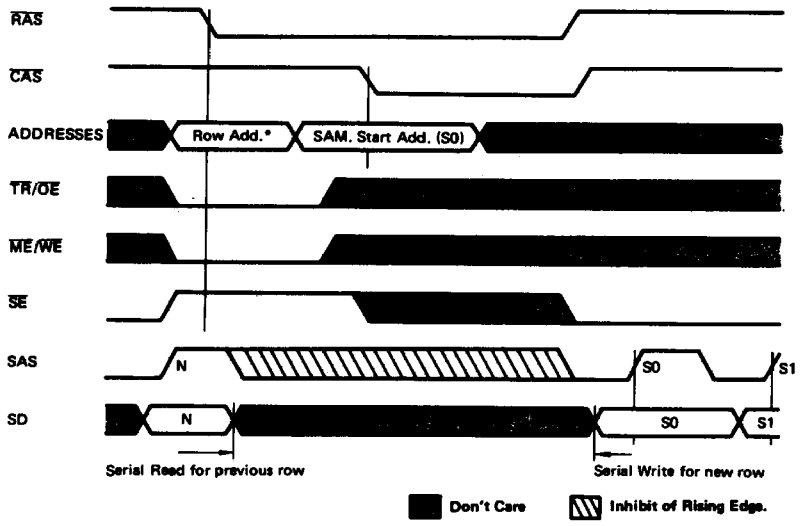
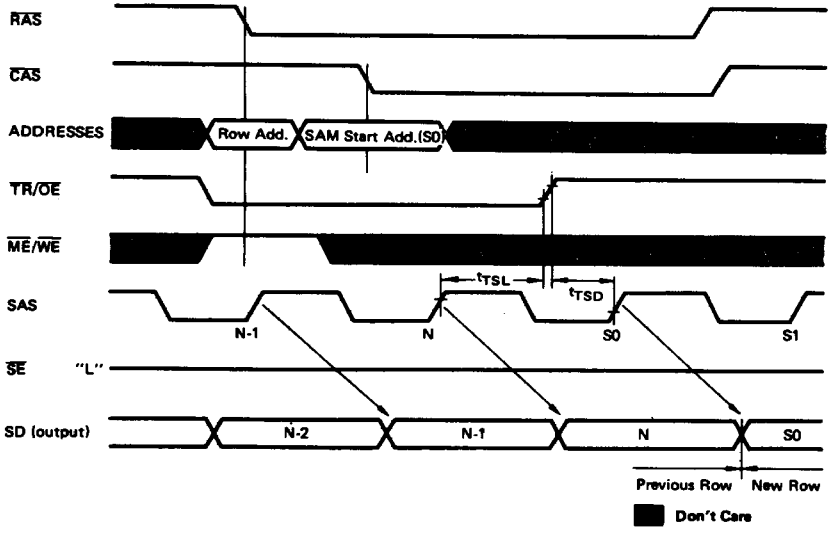
Fig. 3 – EXAMPLE OF PSEUDO WRITE TRANSFER CYCLE



*The DRAM data of this row address are refreshed during pseudo write transfer cycle.

Fig. 4 – EXAMPLE OF REAL TIME READ TRNASFER OPERATION



RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4		6.5	V	
Input Low Voltage	V_{IL}	-2.0		0.8	V	

CAPACITANCE (T_A=25°C)

Paramter	Symbol	Typ	Max		Unit
			DIP	ZIP	
Input Capacitance (A0 to A7)	C_{IN1}		7	8	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{SE}$, $\overline{TR}$/$\overline{OE}$)	C_{IN2}		10	12	pF
Input Capacitance (SAS)	C_{IN3}		7	7	pF
Input/Output Capacitance (MD0/DQ0 to MD3/DQ3)	C_{IO1}		7	8	pF
Input/Output Capacitance (SD0 to SD3)	C_{IO2}		7	8	pF

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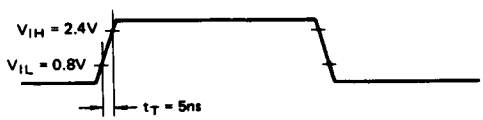
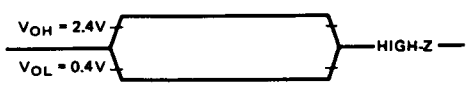
AC TEST CONDITIONS

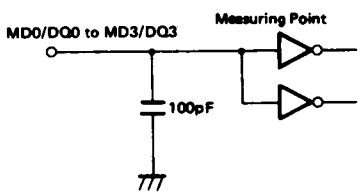
1) Input

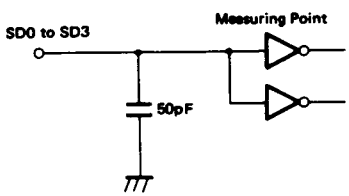


2) Output



3) Output Load





DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
SAM STANDBY $\overline{SE} = V_{IH}$, SAS = V_{IL}					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC1}		95	mA
	MB 81461-15			85	
STANDBY CURRENT Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}		20	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC3}		77	mA
	MB 81461-15			70	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ = cycling, t_{PC} = min)	MB 81461-12	I_{CC4}		50	mA
	MB 81461-15			45	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461-12	I_{CC5}		77	mA
	MB 81461-15			70	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC6}		110	mA
	MB 81461-15			100	
SAM ACTIVE $\overline{SE} = V_{IL}$, t_{SC} = min					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC7}		130	mA
	MB 81461-15			110	
STANDBY CURRENT Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	MB 81461-12	I_{CC8}		50	mA
	MB 81461-15			40	
REFRESH CURRENT 1* Average power supply current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC9}		112	mA
	MB 81461-15			95	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, t_{PC} = min)	MB 81461-12	I_{CC10}		85	mA
	MB 81461-15			70	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461-12	I_{CC11}		112	mA
	MB 81461-15			95	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC12}		145	mA
	MB 81461-15			125	

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
INPUT LEAKAGE CURRENT Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, V_{CC}=5.5V, V_{SS}=0V, all other pins not under test=0V)	$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH}=-5mA/-2mA for DQi/SDi) Output low voltage (I_{OL}=4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V

Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) [redacted]

Parameter [redacted]	Symbol	MB 81461-12		BM 81461-15		Unit
		Min	Max	Min	Max	
Time between Refresh (RAM/SAM)	t_{REF}		4		4	ms
Random Read/Write Cycle Time	t_{RC}	230		260		ns
Read-Modify-Write Cycle Time	t_{RWC}	305		345		ns
Page Mode Cycle Time	t_{PC}	120		145		ns
Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	195		225		ns
Access Time from $\overline{RAS}$ [redacted]	t_{RAC}		120		150	ns
Access Time from $\overline{CAS}$ [redacted]	t_{CAC}		60		75	ns
Output Buffer Turn Off Delay	t_{OFF}	0	25	0	35	ns
Transition Time	t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	90		100		ns
$\overline{RAS}$ Pulse Width	t_{RAS}	120	60000	150	60000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	60		75		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time (Normal cycle)		t_{CPN}	40		50		ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	50		60		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$)		t_{CPR}	25		30		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	60	60000	75	60000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		ns
Column Address Hold Time		t_{CAH}	20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		20		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		ns
Write Command Set Up Time		t_{WCS}	-5		-5		ns
Write Command Hold Time		t_{WCH}	30		35		ns
Write Command Pulse Width		t_{WP}	30		35		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	40		45		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	30		35		ns
Access Time from $\overline{TR}/\overline{OE}$	6	t_{OEA}		35		40	ns
$\overline{TR}/\overline{OE}$ to Data In Delay Time		t_{OED}	25		30		ns

3

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
Output Buffer Turn Off Delay from $\overline{TR}/\overline{OE}$		t_{OEZ}	0	25	0	30	ns
$\overline{TR}/\overline{OE}$ Hold Time Referenced to $\overline{ME}/\overline{WE}$		t_{OEH}	0		0		ns
$\overline{TR}/\overline{OE}$ to $\overline{RAS}$ inactive Set Up Time		t_{OES}	0		0		ns
Data In to $\overline{CAS}$ Delay Time	16	t_{DZC}	0		0		ns
Data In to $\overline{TR}/\overline{OE}$ Delay Time	16	t_{DZO}	0		0		ns
Refresh Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCS}	25		30		ns
Refresh Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCH}	25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	20		20		ns
Serial Clock Cycle Time		t_{SC}	40	50000	60	50000	ns
Access Time from SAS	10	t_{SAC}		40		60	ns
Access Time from $\overline{SE}$	10	t_{SEA}		40		50	ns
SAS Precharge Time		t_{SP}	10		20		ns
SAS Pulse Width		t_{SAS}	10		20		ns
$\overline{SE}$ Precharge Time		t_{SEP}	25		45		ns
$\overline{SE}$ Pulse Width		t_{SE}	25		45		ns
Serial Data Out Hold Time after SAS High		t_{SOH}	10		10		ns
Serial Output Buffer Turn Off Delay from $\overline{SE}$		t_{SEZ}	0	25	0	30	ns
Serial Data In Set Up Time	11	t_{SDS}	0		0		ns
Serial Data In Hold Time	11	t_{SDH}	20		25		ns

3

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{TS}	0		0		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{RTH}	90		110		ns
Write Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time	12	t_{RTHW}	12		15		ns
Transfer Command ($\overline{TR}$) to $\overline{CAS}$ Hold Time		t_{CTH}	30		35		ns
Transfer Command ($\overline{TR}$) to SAS Lead Time		t_{TSL}	5		10		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Lead Time		t_{TRL}	130		140		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Delay Time		t_{TRD}	−65		−50		ns
First SAS Edge to Transfer Command Delay Time		t_{TSD}	25		35		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Set Up Time		t_{WSR}	0		0		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Hold Time		t_{RWH}	12		15		ns
Mask Data (MD) to $\overline{RAS}$ Set Up Time		t_{MS}	0		0		ns
Mask Data (MD) to $\overline{RAS}$ Hold Time		t_{MH}	35		45		ns
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	12	t_{SDZ}	10	60	10	75	ns
Serial Output Buffer Turn On Delay from $\overline{RAS}$	12	t_{SRO}	0		0		ns
SAS to $\overline{RAS}$ Set Up Time	11	t_{SRS}	40		60		ns
$\overline{RAS}$ to SAS Delay Time	12	t_{SRD}	30		45		ns
Serial Data Input to $\overline{SE}$ Delay Time		t_{SZE}	0		0		ns
Serial Data Input Delay from $\overline{RAS}$	12	t_{SDD}	60		75		ns

AC CHARACTERISTICS

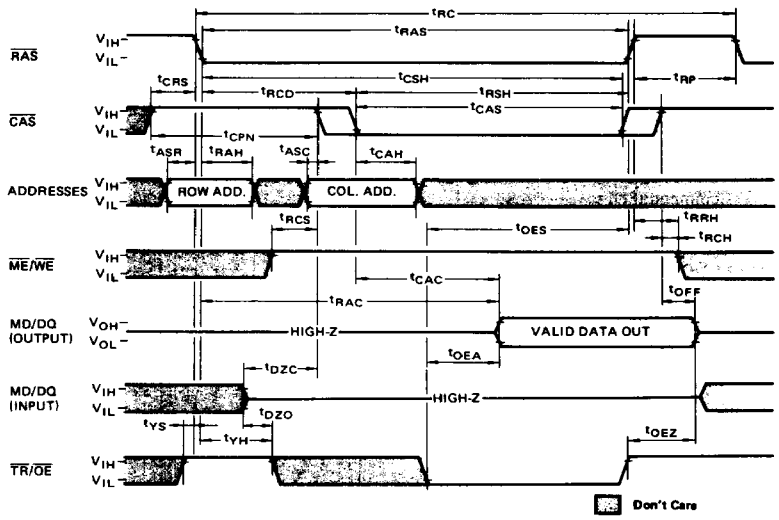
Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
Serial Data Input to $\overline{RAS}$ Delay Time	13	t_{SZS}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Set up Time	14	t_{ESR}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	14	t_{REH}	12		15		ns
Serial Write Enable Set up Time	11	t_{SWS}	20		30		ns
Serial Write Enable Hold Time	11	t_{SWH}	80		120		ns
Serial Write Disable Set Up Time	11	t_{SWIS}	20		30		ns
Serial Write Disable Hold Time	11	t_{SWIH}	40		60		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{YS}	0		0		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{YH}	12		15		ns
Time between Transfer	15	t_{REFT}		4		4	ms

NOTES;

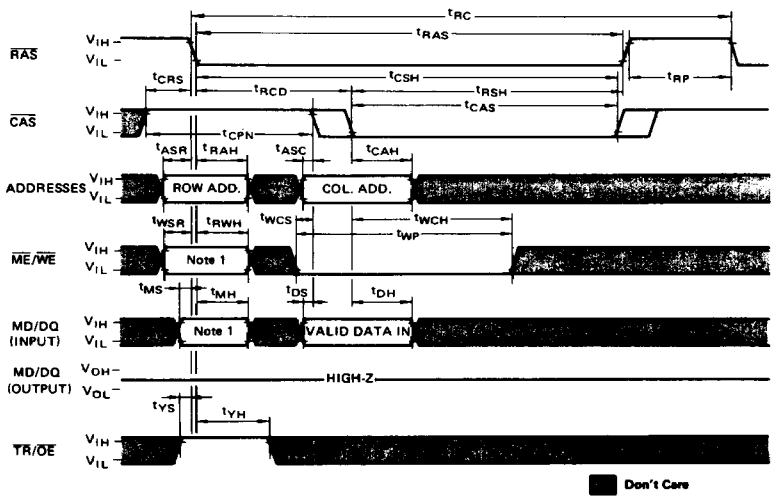
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 transfer, and 8 SAS cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycle are required
2. AC characteristics assume
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Measured with a load equivalent to 2 TTL loads and 50pF.
11. Input mode only
12. Write transfer and pseuso write transfer only.
13. Read transfer only in the case that the previous transfer was write transfer.
14. Pseudo write transfer only.
15. If t_{REFT} is not satisfied, 8 transfer and 8 SAS cycles before proper device operation is needed.
16. Either t_{DZC} or t_{DZO} must be satisfied.

3

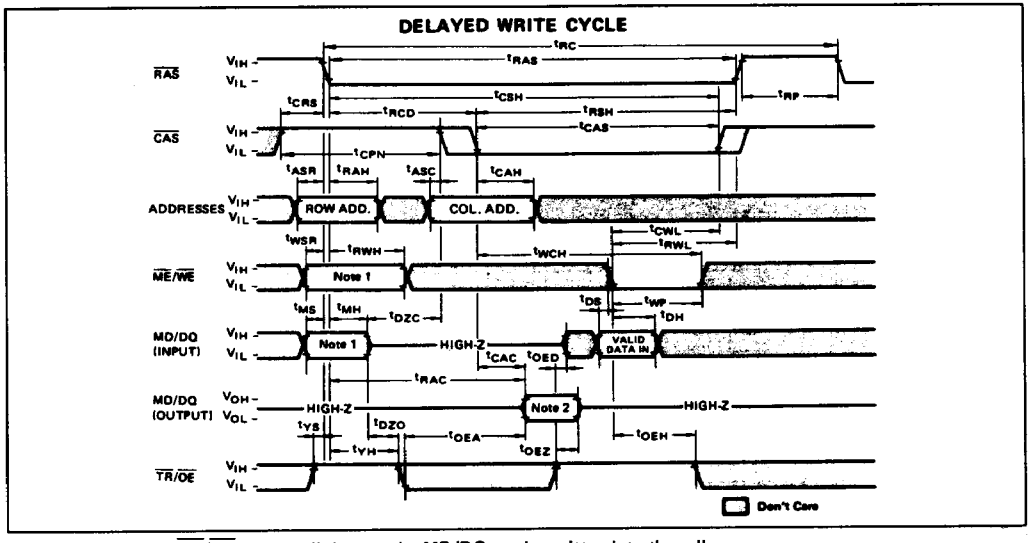
READ CYCLE



WRITE CYCLE (EARLY WRITE)

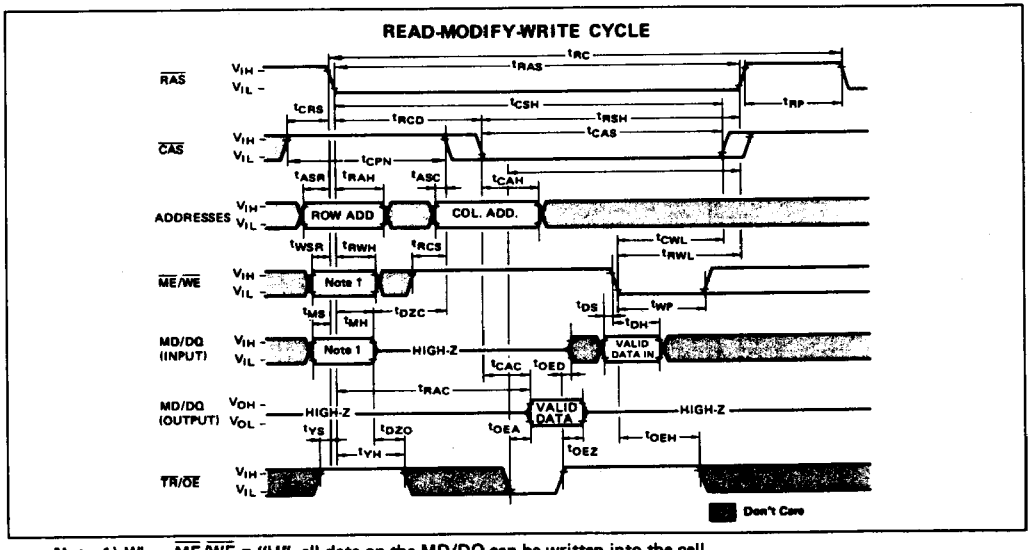


Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.



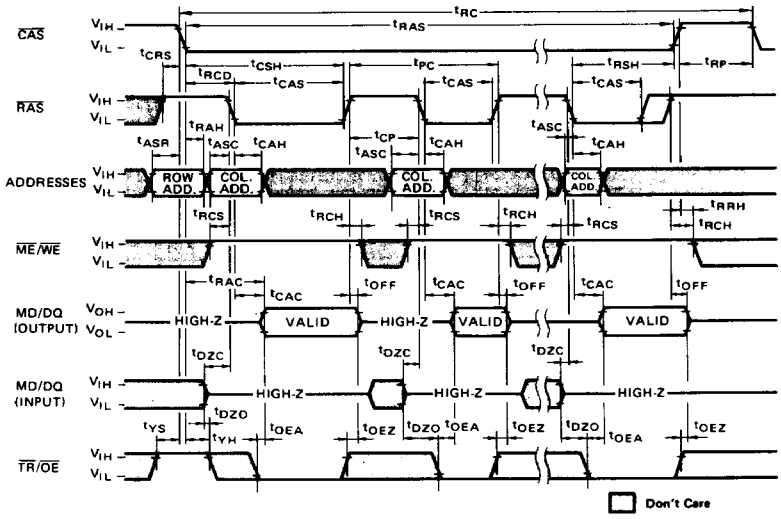
Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

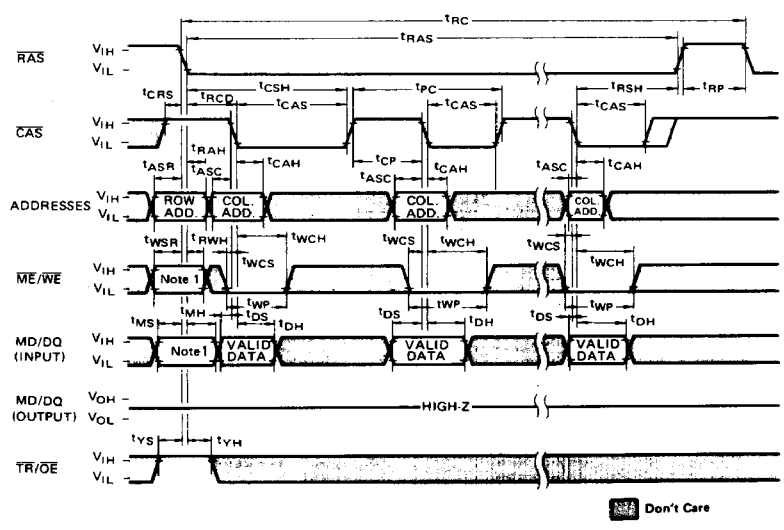


Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

PAGE MODE READ CYCLE

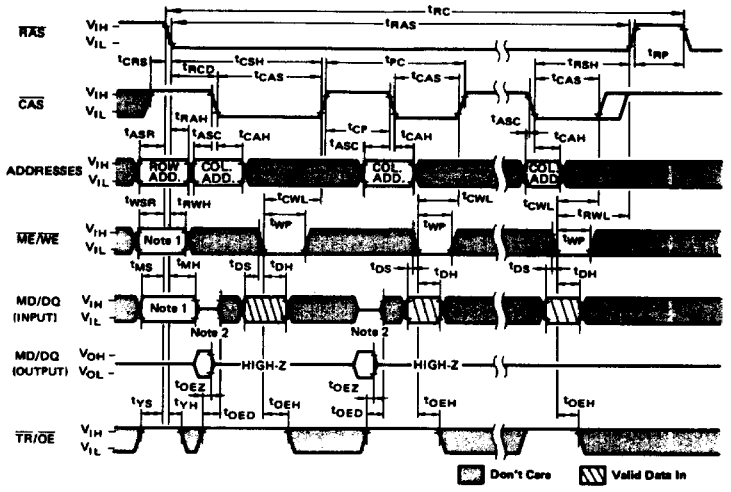


PAGE MODE WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

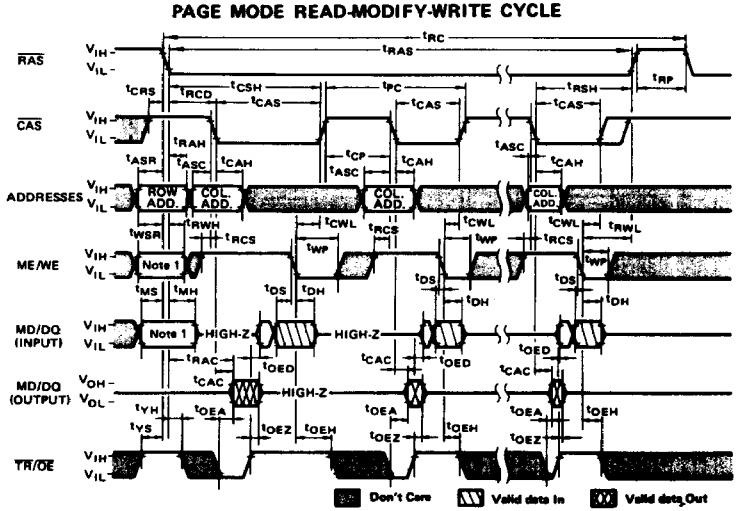
PAGE MODE DELAYED WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

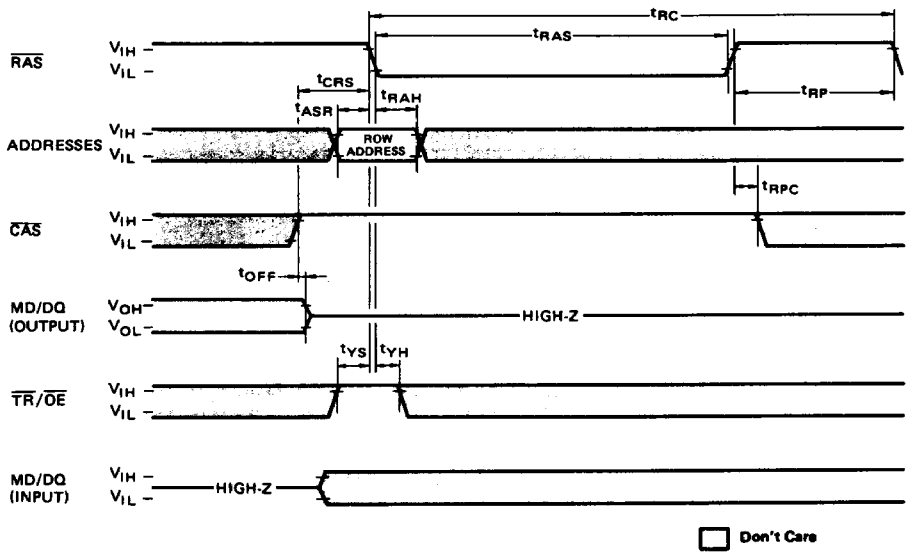
PAGE MODE READ-MODIFY-WRITE CYCLE



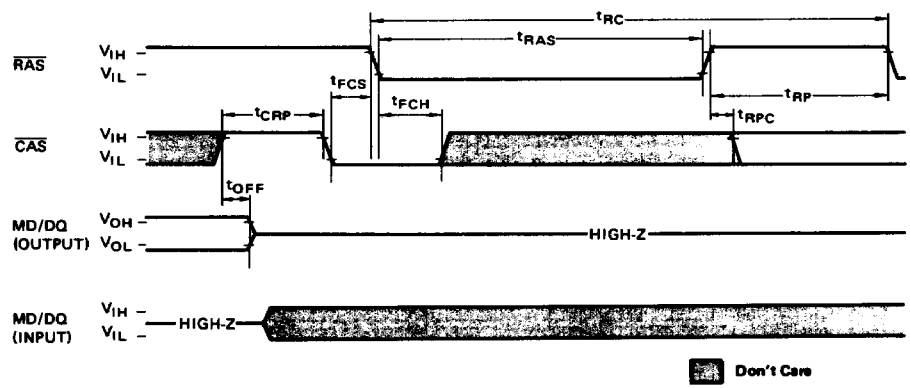
Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

3

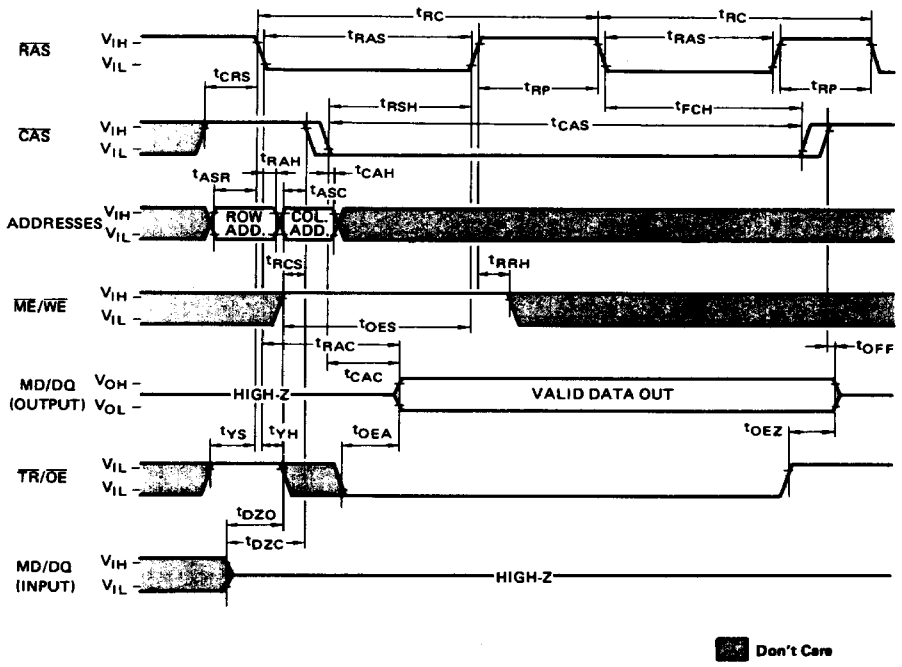
$\overline{RAS}$-ONLY REFRESH CYCLE ($\overline{ME}/\overline{WE}$=Don't Care)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (ADDRESS, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$=Don't Care)

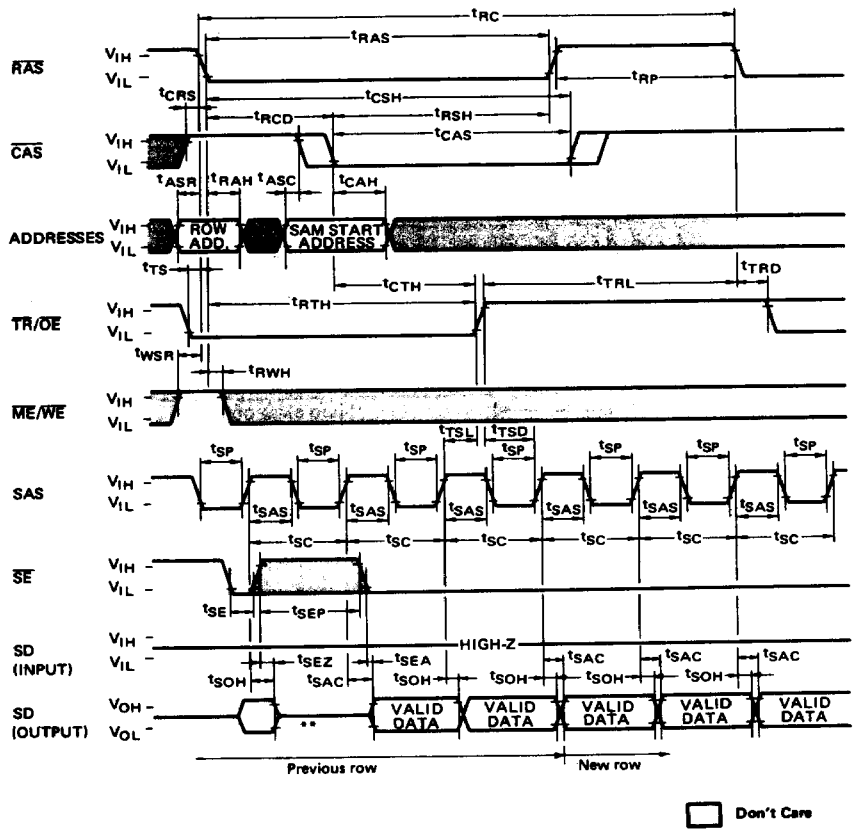


HIDDEN REFRESH CYCLE



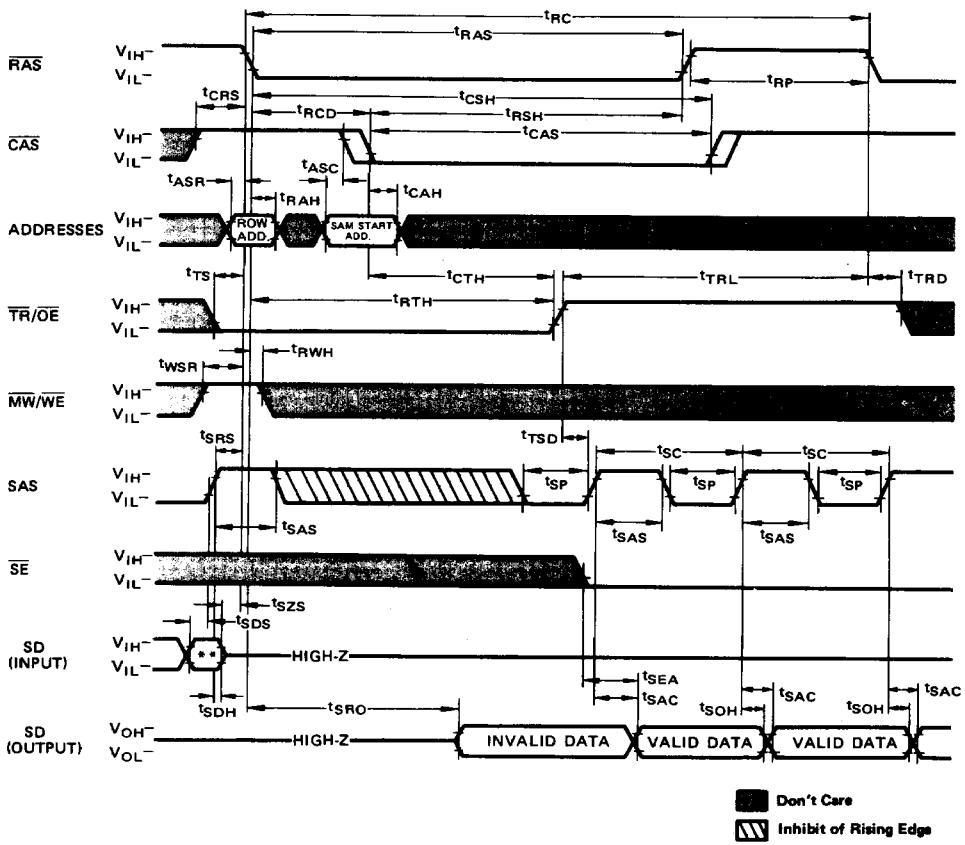
3

READ TRANSFER CYCLE* (MD/DQ = Don't Care)



*: In the case that the previous transfer is read transfer.
**: If $\overline{SE}$ is low, the valid data will appear within t_{SAC} or t_{SEA}.

READ TRANSFER CYCLE* (MD/DQ = Don't Care)

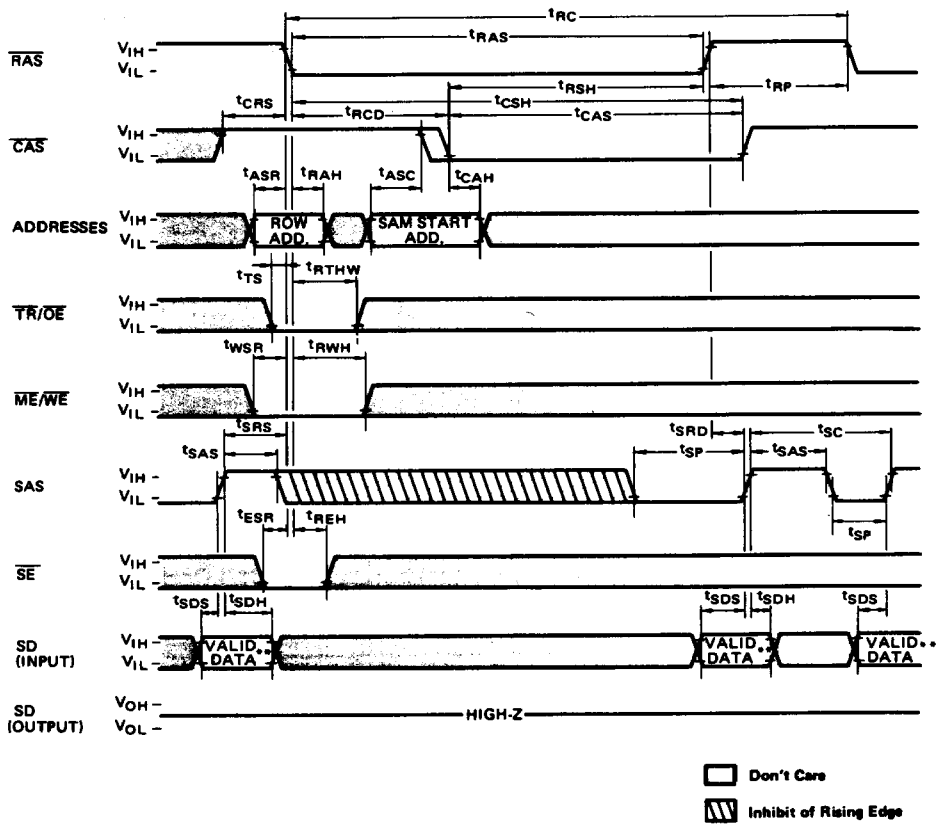


*; In the case that the previous transfer is write transfer.

**; If $\overline{SE}$ is low and the previous cycle is serial write cycle, this should be valid data input.

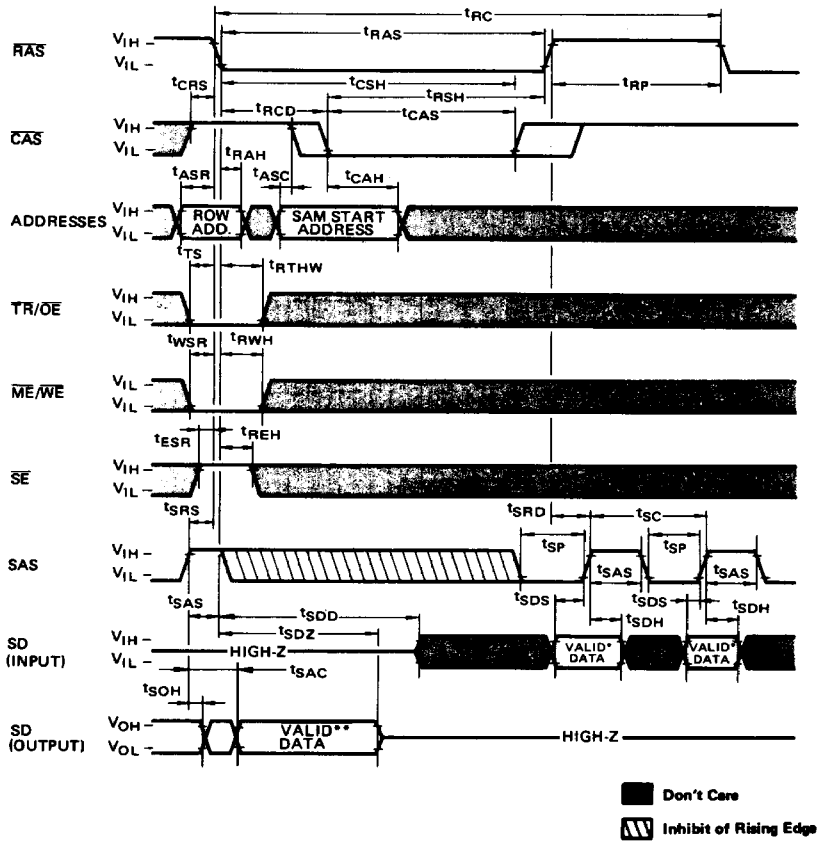
3

WRITE TRANSFER CYCLE* (MD/DQ = Don't Care)



*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is high these data are not written into the SAM.

PSEUDO WRITE TRANSFER CYCLE (MD/ DQ = Don't Care)

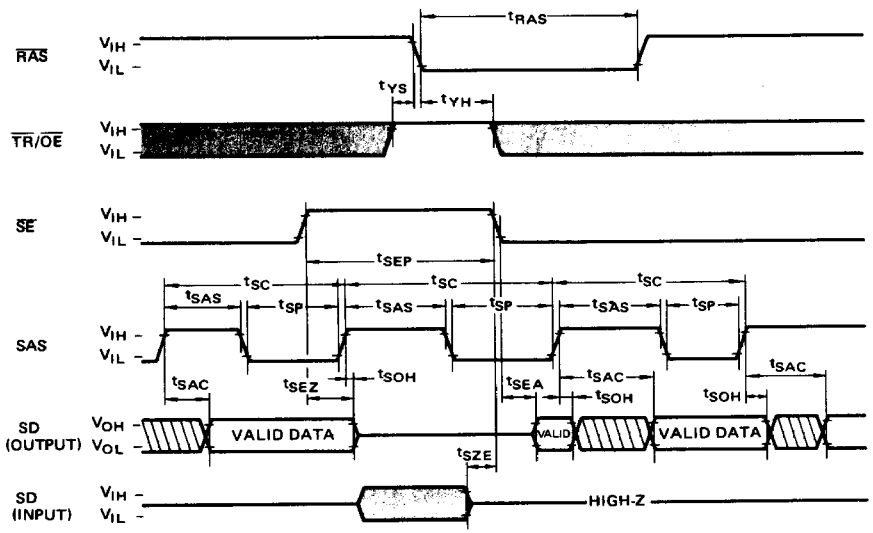


*: If $\overline{SE}$ is high, these data are not written into SAM.
**: If $\overline{SE}$ is high, SD (SD0 to SD3) are in High-Z state after t_{SEZ}.
If $\overline{SE}$ becomes low, the valid data will appear meeting t_{SAC} and t_{SEA}.

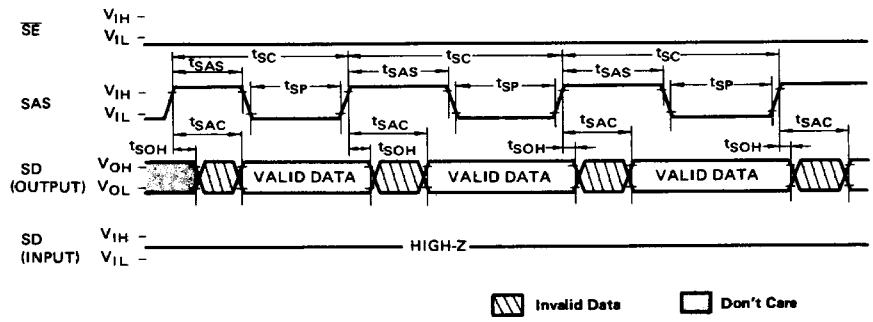
3

3

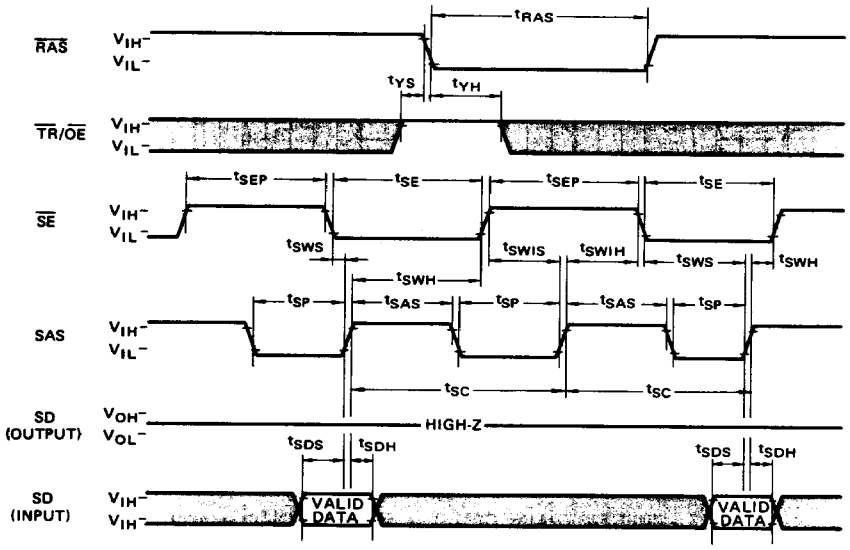
SERIAL READ CYCLE



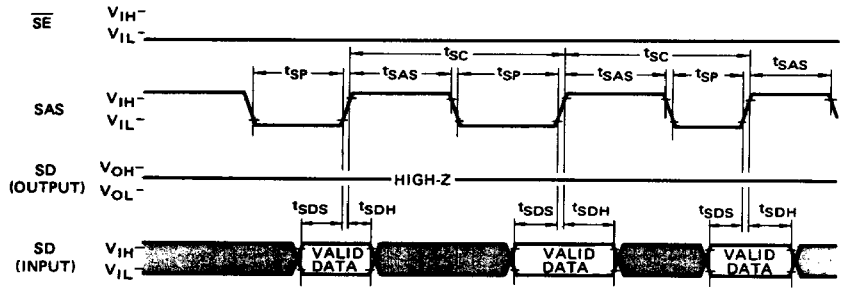
In the case of $\overline{SE}$="L" while the operation;



SERIAL WRITE CYCLE



In the case of $\overline{SE}$="L" while the operation;



Don't Care

3

Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

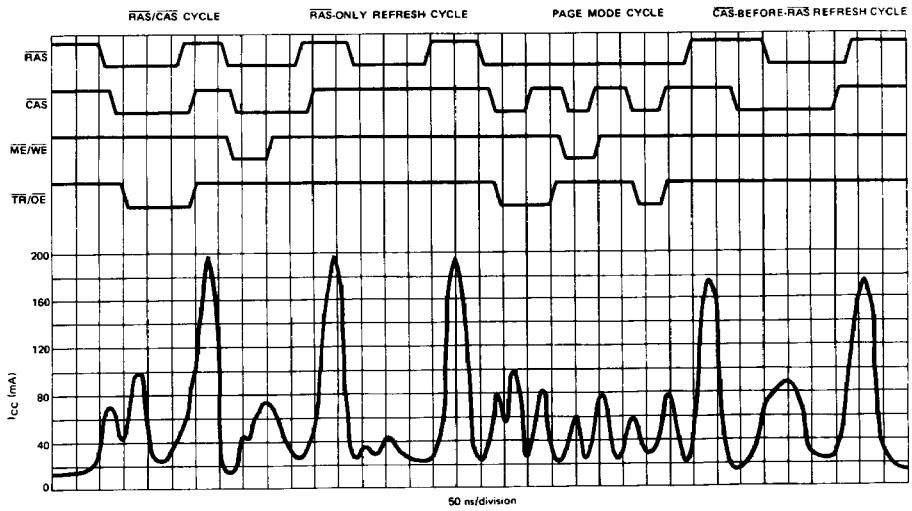
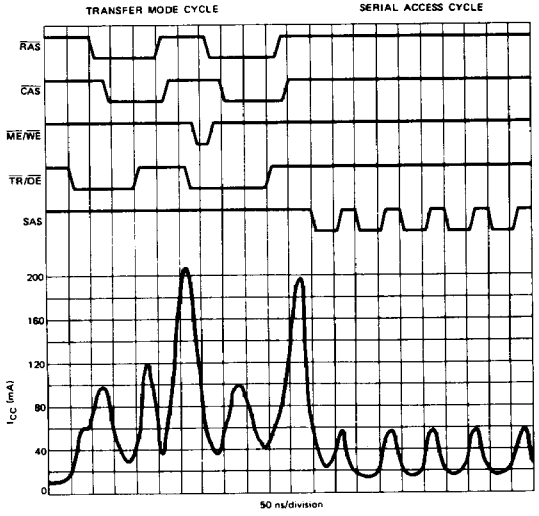


Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C) (cont'd)



TYPICAL CHARACTERISTICS CURVES

Fig. 6 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

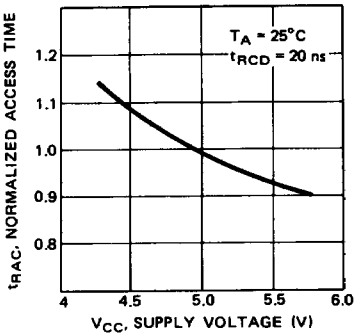


Fig. 7 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

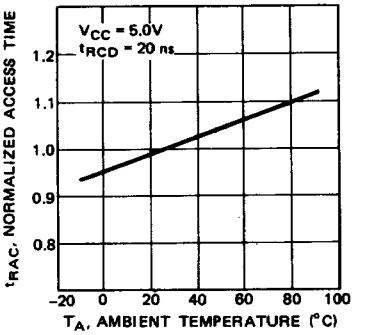


Fig. 8 – OPERATING CURRENT vs CYCLE RATE

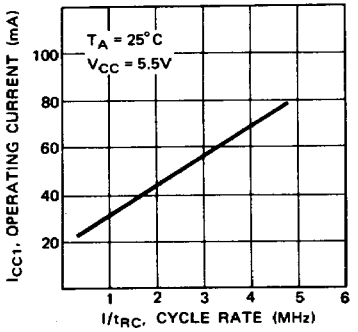


Fig. 9 – OPERATING CURRENT vs SUPPLY VOLTAGE

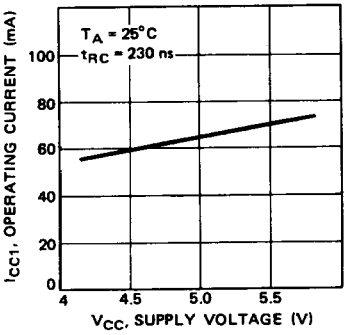


Fig. 10 – OPERATING CURRENT vs AMBIENT TEMPERATURE

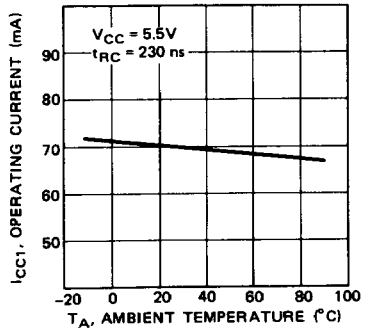


Fig. 11 – STANDBY SURRENT vs SUPPLY VOLTAGE

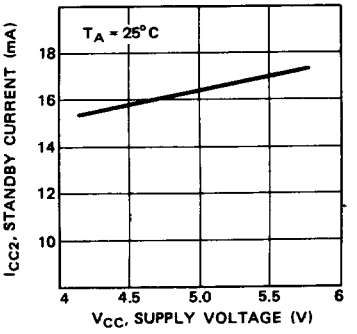


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Fig. 12 – STANDBY CURRENT vs AMBIENT TEMPERATURE

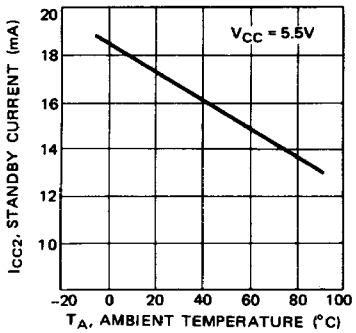

Fig. 13 – REFRESH CURRENT 1 vs CYCLE RATE

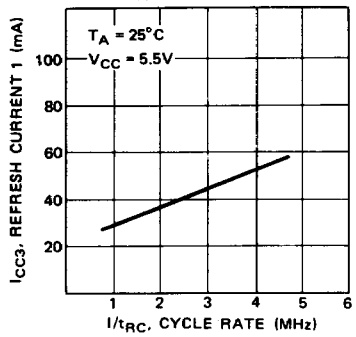

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Fig. 14 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

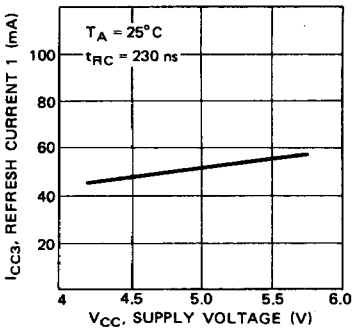

Fig. 15 – PAGE MODE CURRENT vs CYCLE RATE

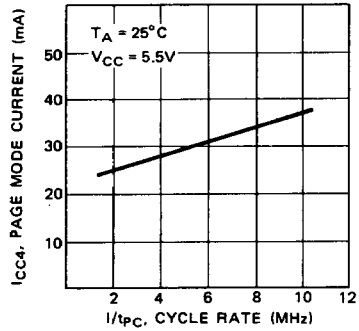

Fig. 16 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

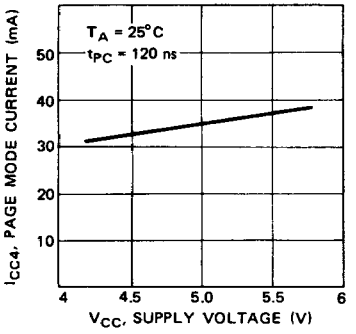

Fig. 17 – REFRESH CURRENT 2 vs CYCLE RATE

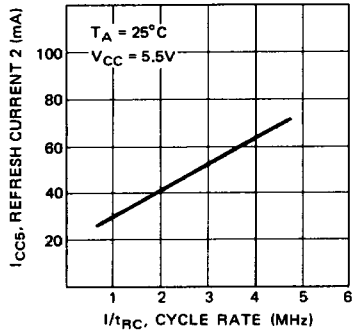

Fig. 18 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

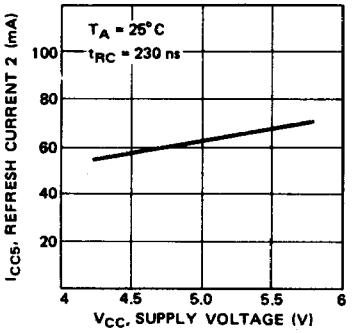

Fig. 19 – TRANSFER MODE CURRENT vs CYCLE RATE

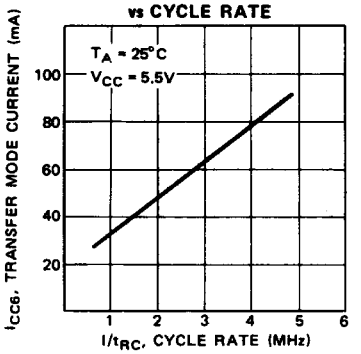

Fig. 20 – TRANSFER MODE CURRENT vs SUPPLY VOLTAGE

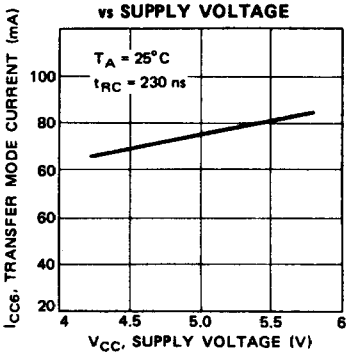

Fig. 21 – RAM STANDBY/SAM ACTIVE CURRENT vs CYCLE RATE

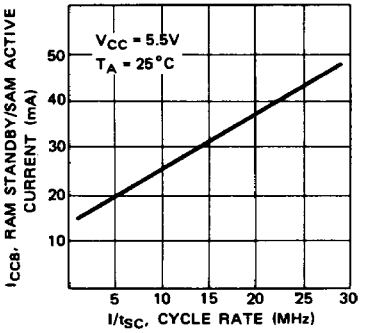

Fig. 22 – RAM STANDBY/SAM ACTIVE CURRENT vs SUPPLY VOLTAGE

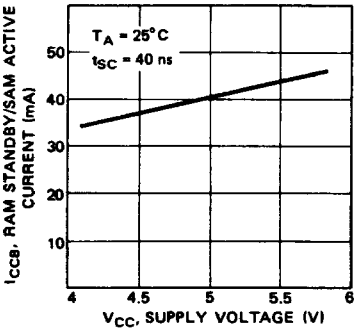

Fig. 23 – RAM STANDBY/SAM ACTIVE CURRENT vs AMBIENT TEMPERATURE

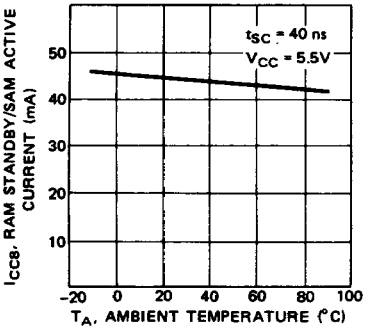

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Fig. 24 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

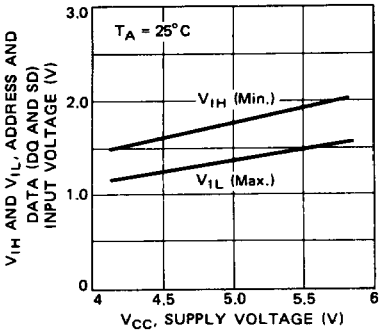

Fig. 25 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

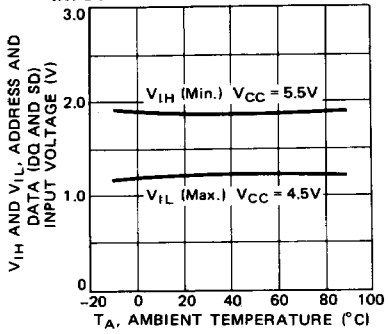

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Fig. 26 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs SUPPLY VOLTAGE

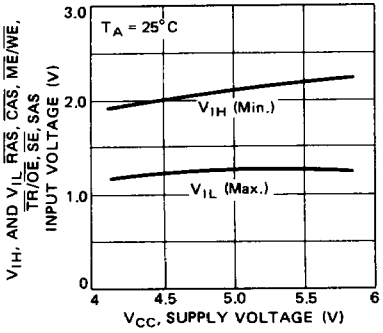


Fig. 27 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs AMBIENT TEMPERATURE

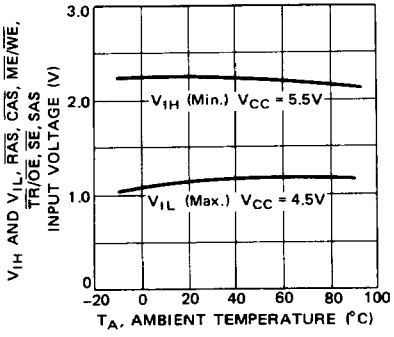


Fig. 28 – ACCESS TIME (RAM) vs LOAD CAPACITANCE

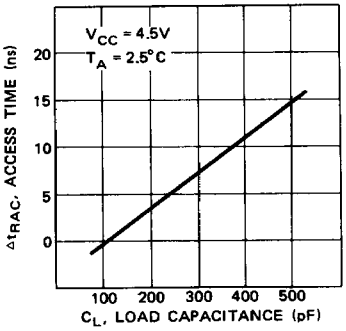


Fig. 29 – ACCESS TIME (SAM) vs LOAD CAPACITANCE

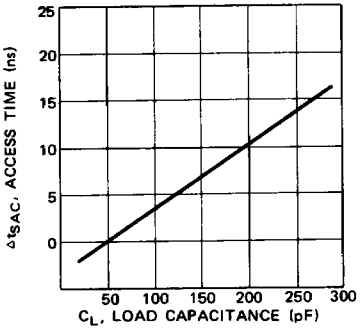


Fig. 30 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

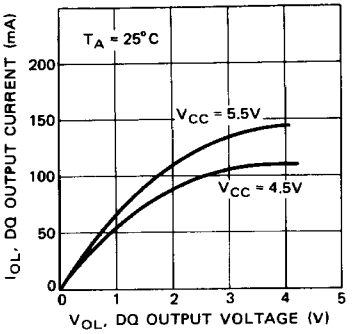


Fig. 31 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

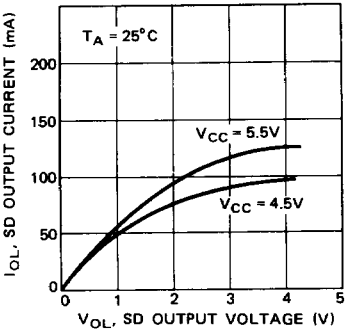


Fig. 32 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

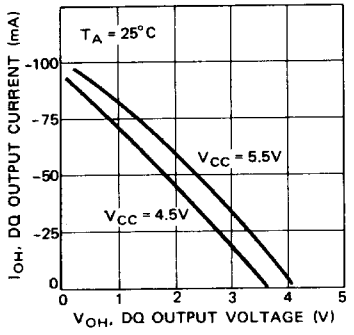


Fig. 33 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

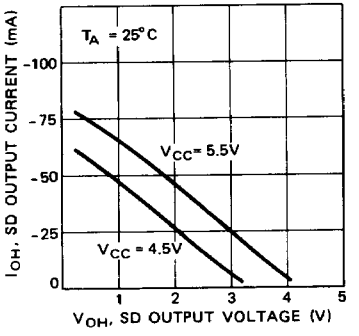
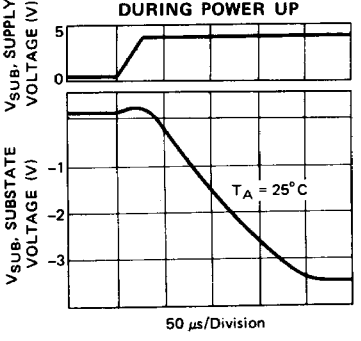


Fig. 34 – SUBSTRATE VOLTAGE DURING POWER UP



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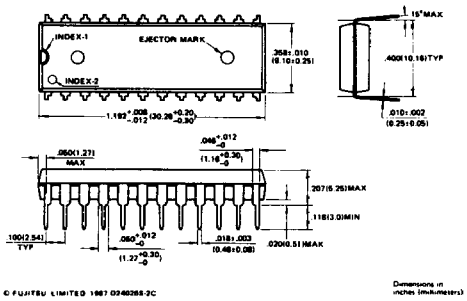
PACKAGE DIMENSIONS

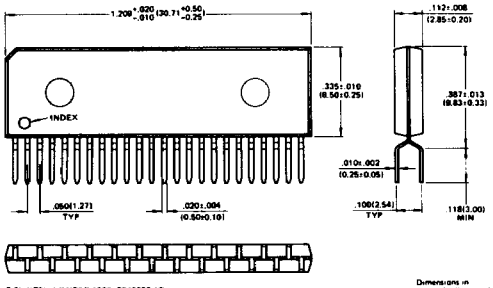
PLASTIC DIP (Suffix: -P) PLASTIC ZIP (Suffix: -PSZ)

24-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-24P-M04)



Dimensions in inches (millimeters)

24-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-24P-M02)



Dimensions in inches (millimeters)

3