M5M410092FP,RF-10,-13,-15

10485760-BIT(327680-WORD BY 32-BIT) FRAME BUFFER MEMORY

DESCRIPTION

The M5M410092FP,RF is a 10M-bit Frame Buffer memory which integrates a 327680-word by 32-bit dynamic RAM array, 2048-bit triple-port static RAM as a pixel buffer, dual 640-bit wide serial access memory (SAM) and pixel ALU. Dynamic RAM array is connected to a pixel buffer by a 256-bit global bus. The buffer is linked to an on-board pixel ALU by 32-bit read and write ports. The ports operate concurrently with the dynamic RAM array on the internal bus.

Within its on-chip pixel ALU, the M5M410092FP, RF is able to convert Z-buffer operations and pixel blends from "read-modify-writes" to "mostly writes", thereby completing data modifications in one pixel buffer clock cycle and reducing execution time by up to 75 percent. The pixel ALU has four 8-bit ROP units, four 8-bit blend units, one 32-bit match comparator, and one 32-bit magnitude comparator.

The dynamic RAM array is comprised of four independent, interleaved 2.5M DRAM banks with each pair of banks sharing a 640-bit wide, SAM video buffer. The video buffers can achieve a 76 Hz refresh rate as one can be loaded while the other is sending out video data.

The on-board pixel buffer can hold up to eight blocks of data, each containing 256-bits, and has cycle times of 10, 13 and 15ns. With the 256-bit global bus operating as its maximum speed of 20 ns and transferring 32-byte blocks, data can be moved from the DRAM banks to the pixel buffer at a rate of up to 1.6Gbyte/sec.

The M5M410092FP,RF is fabricated with a high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation,and low costs are essential. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs.

FEATURES

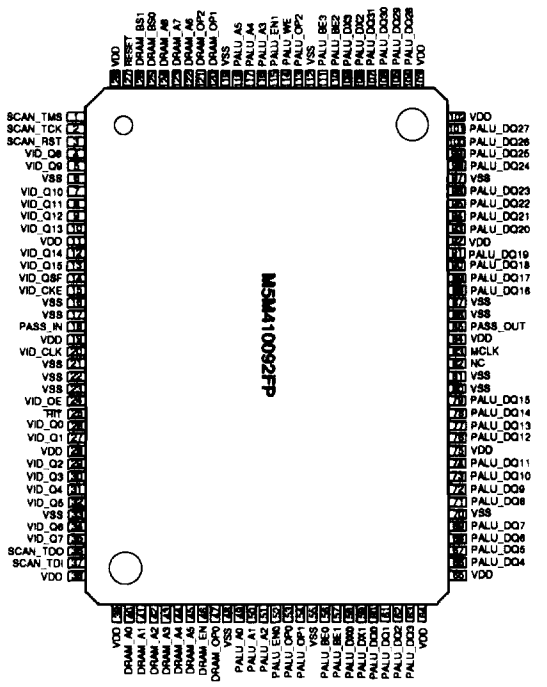
Type name	Pixel Buffer Read Access/ Cycle (ns)	Pixel Buffer Write Cycle (ns)	Serial Read Access/ Cycle (ns)	Block Transfer Cycle (ns)
M5M410092FP,RF-10	14/20	10	10/14	20
M5M410092FP,RF-13	20/26	13	10/14	26
M5M410092FP,RF-15	24/30	15	10/14	45

- 10M-bit DRAM array
  - Four independent, interleaved 2.5M banks
  - 1280 x 1024 x 8-bit image supported
- Two 640-bit wide SAM video buffer
  - One for each DRAM bank
  - Simultaneous operation/Up to 76Hz refresh rate
- 256-bit global bus, 1.6Gbyte/sec
- 32-bit pixel buffer/ALU read and write ports
- 2048-bit pixel buffer
  - Up to eight 256-bit data blocks
  - 10ns, 13ns, and 15ns average cycle times
  - Up to 1.6Gbyte/sec transfer rate with bus moving 32-byte blocks at 20ns pipelined architectur
- Pixel ALU
  - Converts Z-buffer operation to mostly write
  - Completes modifications in one pixel buffer cycle
  - Four 8-bit ROP units/Four 8-bit blend units
  - One 32-bit magnitude comparator/One 32-bit match comparator
- Second-generation, 0.5 μm CMOS technology
- 128-pin, plastic QFP
- Single 3.3V ±5% supply

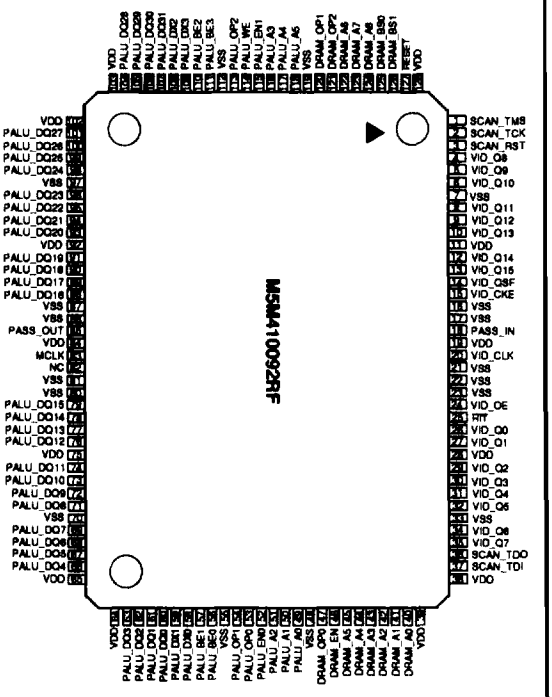
APPLICATION

High-performance engineering workstations, Video arcade games, Flight simulators/sophisticated simulation applications, Virtual reality

PIN CONFIGURATION (TOP VIEW)



Outline 128P6D-C (128 pin QFP Normal Bend Type)



Outline 128P6D-D (128 pin QFP Reverse Bend Type)

NC: NO CONNECTION

Pin name	Function
MCLK	Master clock
$\overline{\text{RESET}}$	Reset
PALU_EN	Enable Pixel ALU operation starting next cycle
PALU_WE	Pixel ALU write enable
PALU_OP	Pixel ALU opcode
PALU_A	Read/Write address
PALU_BE	Byte write or output enables
PALU_DQ	data pins
PALU_DX	Data extension pins for blending
PASS_OUT	Compare output
PASS_IN	Compare input
$\overline{\text{HIT}}$	Picking logic flag output
DRAM_EN	Enable DRAM operation at next cycle
DRAM_OP	DRAM opcode
DRAM_BS	DRAM bank select
DRAM_A	Address for page, block and video line

Pin name	Function
VID_CLK	Video clock
VID_CKE	Video clock enable
VID_OE	Video output enable
VID_Q	Video data bus
VID_QSF	Video buffer indicator
SCAN_RST	Scan reset
SCAN_TCK	Scan clock
SCAN_TMS	Scan test mode select
SCAN_TDI	Scan test data input
SCAN_TDO	Scan test data output
Vss	Ground
VDD	Power supply

BLOCK DIAGRAM