

SILICON GATE CMOS

8,192 WORD x 8 BIT CMOS STATIC RAM

Description

The TC5588P/J is a 65,536 bit high speed CMOS static random access memory organized as 8,192 words by 8 bits and operated from a single 5V supply. Toshiba's advanced CMOS technology and circuit design enable high speed operation.

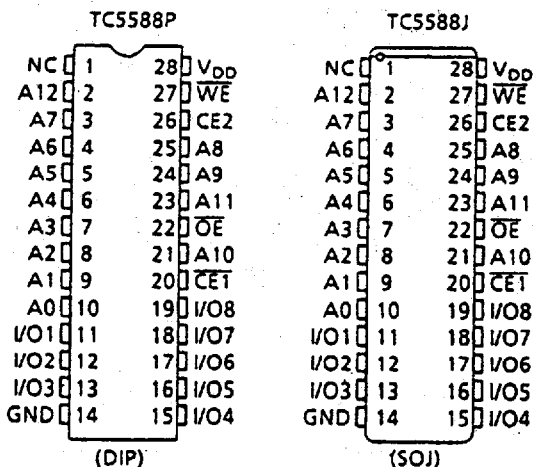
The TC5588P/J features low power dissipation when the device is deselected using chip enable ($\overline{CE1}$, $CE2$) and has an output enable input (\overline{OE}) for fast memory access. Also, the device power between memory accesses is reduced by an automatic power down circuit.

The TC5588P/J is suitable for use in high speed applications such as cache memory and high speed storage. All inputs and outputs are TTL compatible. The TC5588P/J is available in a 300mil width, 28-pin DIP and SOJ suitable for high density surface assembly.

Features

- Fast access time
 - TC5588P/J-15 15ns (max.)
 - TC5588P/J-20 20ns (max.)
 - TC5588P/J-25 25ns (max.)
 - TC5588P/J-35 35ns (max.)
- Low power dissipation
 - Operation:
 - TC5588P/J-15 135mA (max.)
 - TC5588P/J-20 115mA (max.)
 - TC5588P/J-25 115mA (max.)
 - TC5588P/J-35 115mA (max.)
 - Standby: 1mA (max.)
- Single 5V power supply: $5V \pm 10\%$
- Fully static operation
- Inputs and outputs TTL compatible
- Output buffer control: \overline{OE}
- Package:
 - TC5588P: DIP28-P-300B
 - TC5588J: SOJ28-P-300A

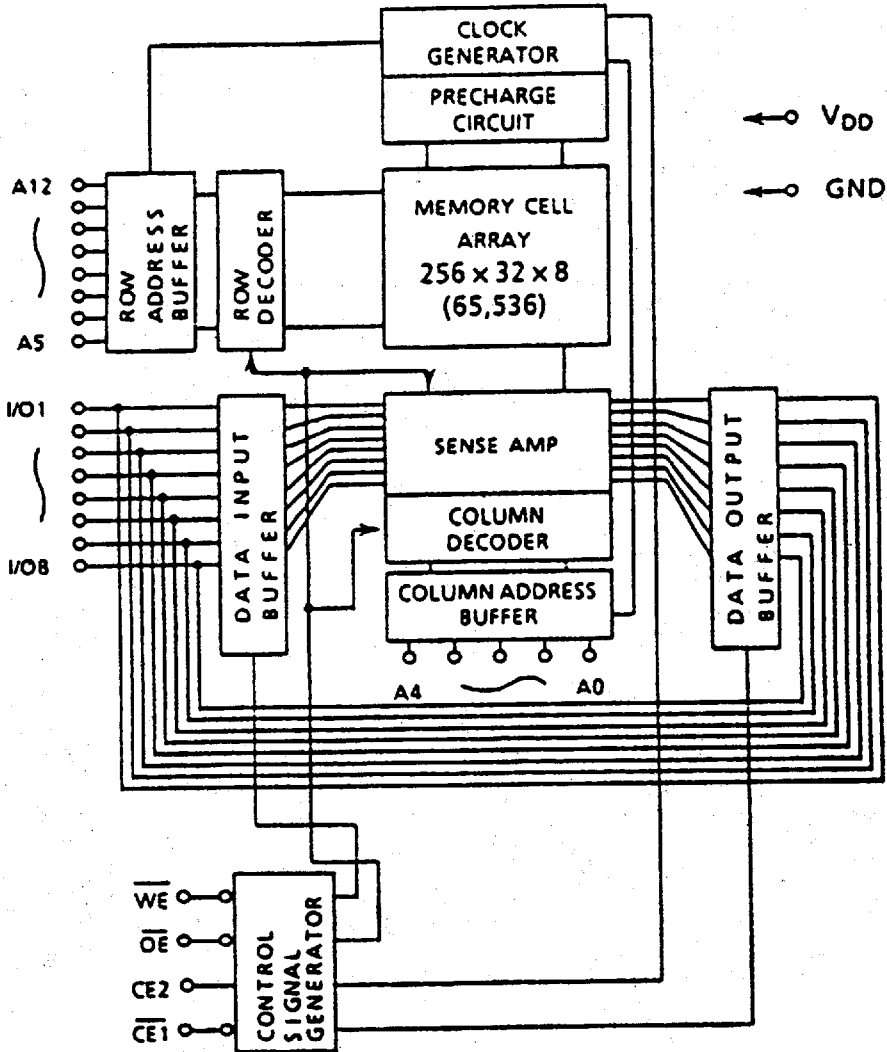
Pin Connection (Top View)



Pin Names

A0 ~ A12	Address Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
$\overline{CE1}$, $CE2$	Chip Enable Inputs
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
NC	No Connection

Block Diagram



Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V _{IN}	Input Voltage	-2.0 ~ 7.0	V
V _{IO}	Input/Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T _{STRG}	Storage Temperature	-65 ~ 150	°C
T _{OPR}	Operating Temperature	-10 ~ 85	°C

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DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	$V_{DD} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5*	-	0.8	V

* -3V with a pulse width of 10ns

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	-	± 1	μA	
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	-	-	± 1	μA	
I_{OH}	Output High Current	$V_{OH} = 2.4V$	-4	-	-	mA	
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	8	-	-	mA	
I_{DDO}	Operating Current	$V_{DD} = 5.5V$ $t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ Other Inputs = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$	-15	-	-	135	mA
			-20	-	-	115	
			-25	-	-	115	
			-35	-	-	115	
I_{DDS1}	Standby Current	$V_{DD} = 5.5V$ $t_{\text{cycle}} = \text{Min cycle}$ $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ Other Inputs = V_{IH}/V_{IL}	-	-	-	25	mA
I_{DDS2}^*		$\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$ Other Inputs = $V_{DD} - 0.2V$ or $0.2V$	-	-	-	1	

* If $\overline{CE1} \geq V_{DD} - 0.2V$, the specified limits are guaranteed under the condition $CE2 \geq V_{DD} - 0.2V$ or $CE2 \leq 0.2V$.

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	7	pF

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C⁽¹⁾, V_{DD} = 5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	15	-	20	-	25	-	35	-	ns
t _{ACC}	Address Access Time	-	15	-	20	-	25	-	35	
t _{CO1}	$\overline{CE1}$ Access Time	-	15	-	20	-	25	-	35	
t _{CO2}	CE2 Access Time	-	15	-	20	-	25	-	35	
t _{OE}	\overline{OE} Access Time	-	9	-	10	-	12	-	12	
t _{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	5	-	
t _{COE}	Output Enable Time from $\overline{CE1}$ or CE2	5	-	5	-	5	-	5	-	
t _{COD}	Output Disable Time from $\overline{CE1}$ or CE2	-	6	-	6	-	6	-	6	
t _{OEE}	Output Enable Time from \overline{OE}	0	-	0	-	0	-	0	-	
t _{ODO}	Output Disable Time from \overline{OE}	-	5	-	5	-	5	-	5	
t _{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	0	-	
t _{PD}	Chip Deselection to Power Down Time	-	15	-	20	-	25	-	35	

Write Cycle

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	15	-	20	-	25	-	35	-	ns
t _{CW}	Chip Enable to End of Write	12	-	13	-	15	-	15	-	
t _{AS}	Address Setup Time	0	-	0	-	0	-	0	-	
t _{WP}	Write Pulse Width	12	-	13	-	15	-	15	-	
t _{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	
t _{DS}	Data Setup Time	9	-	10	-	12	-	12	-	
t _{DH}	Data Hold Time	0	-	0	-	0	-	0	-	
t _{OE_W}	Output Enable Time from \overline{WE}	0	-	0	-	0	-	0	-	
t _{OD_W}	Output Disable Time from \overline{WE}	-	6	-	6	-	6	-	6	

AC Test Conditions

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

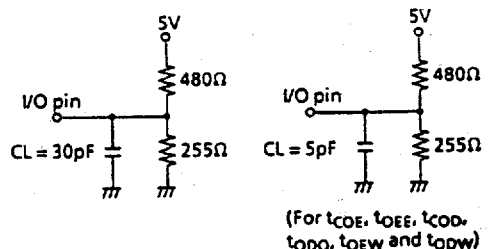
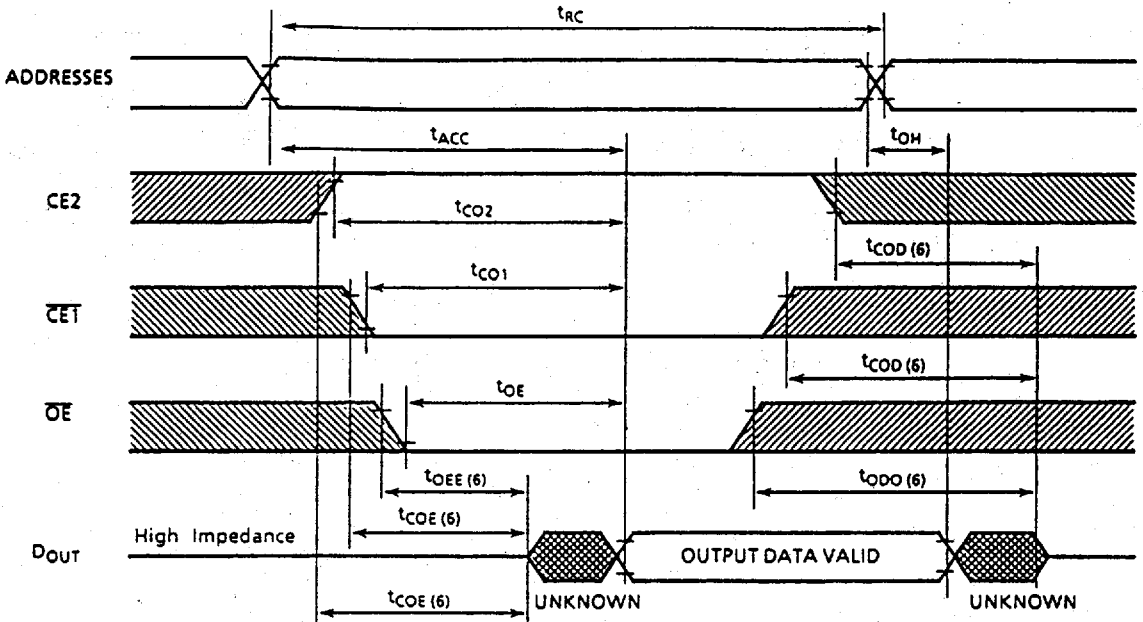


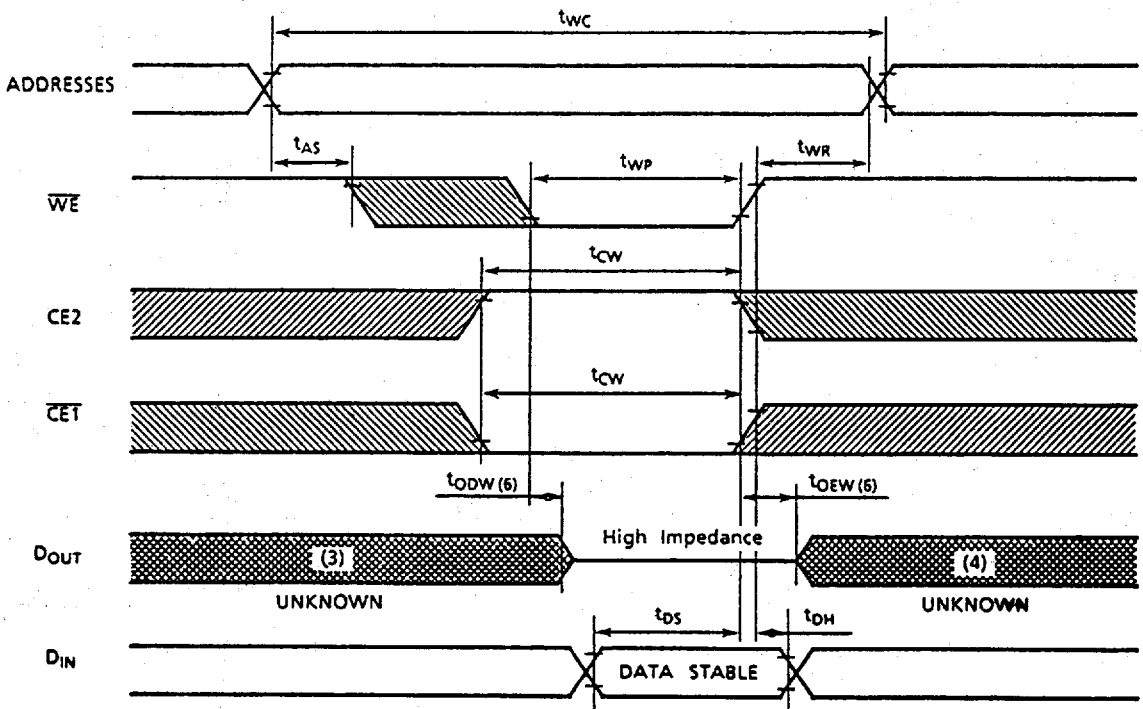
Figure 1.

Timing Waveforms

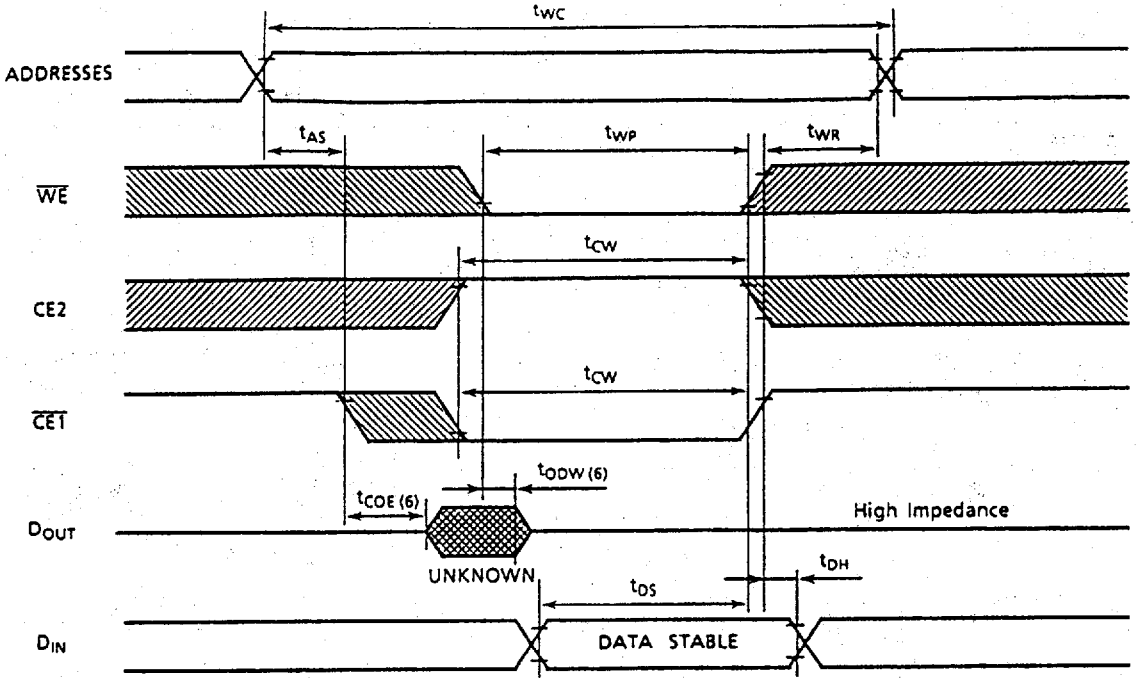
Read Cycle ⁽²⁾



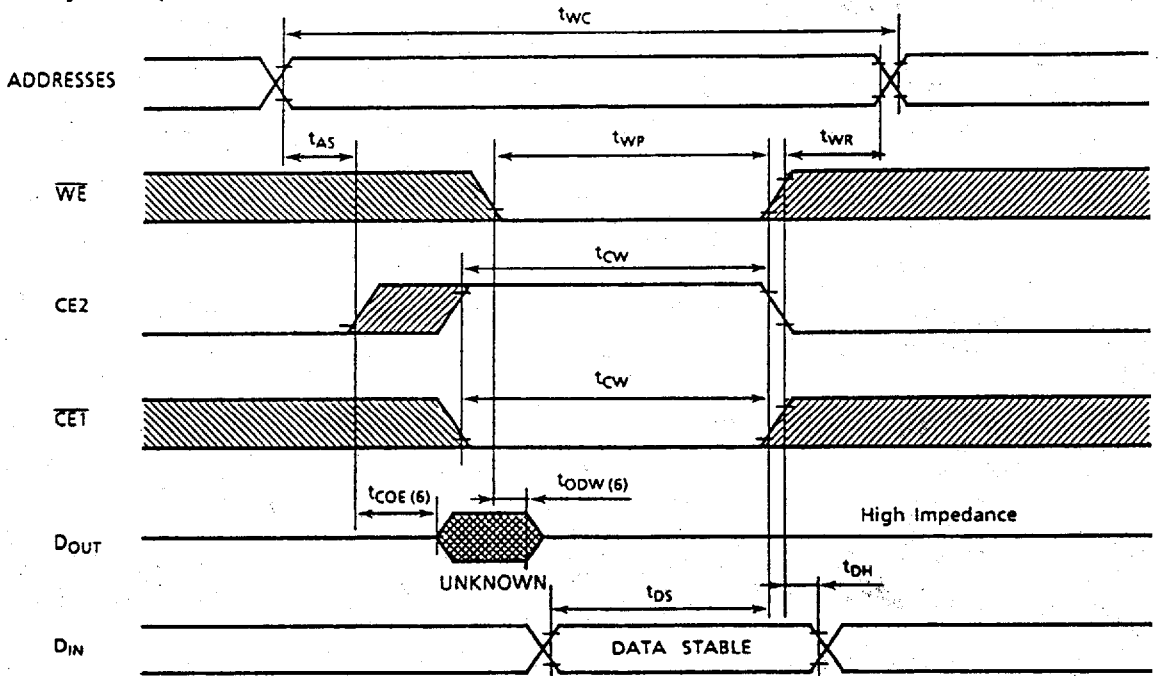
Write Cycle 1 ⁽⁵⁾ (\overline{WE} Controlled Write)



Write Cycle 2 ⁽⁵⁾ ($\overline{CE1}$ Controlled Write)



Write Cycle 3 ⁽⁵⁾ ($\overline{CE2}$ Controlled Write)



Notes:

1. The operating temperature (T_a) is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. \overline{WE} is high for read cycles.
3. If the $\overline{CE1}$ low transition or $CE2$ high transition occurs coincident with or after the \overline{WE} low transition, outputs remain in a high impedance state.
4. If the $\overline{CE1}$ high transition or $CE2$ low transition occurs coincident with or prior to the \overline{WE} high transition, outputs remain in a high impedance state.
5. If \overline{OE} is high during a write cycle, the outputs are in a high impedance state during this period.
6. The following parameters are measured using the load shown in Fig. 1.
 - (A) t_{COE} , t_{OEE} , $t_{OE\overline{W}}$ Output Enable Time
 - (B) t_{COD} , t_{ODO} , $t_{OD\overline{W}}$ Output Disable Time

