MJX440/MJX330
MjxCfg
User's Manual

Rev.2.30 20/02/2004

Document History

Version	contents	data
2.10	・Add a setup of Flash	07/12/2001
2.11	・Modify wrong words	19/12/2001
2.12	・Modify a term（I/F→Interface）	09/01/2002
2.20	・Alter a section for MIPS/EJTAG2.6. ・Add a setup screen	16/04/2003
2.22	・Alter a section for VR5500（Added a setup screen） ・Modify a setup screen of NB85E ・Modify a setup screen of MJX330	20/08/2003
2.23	・Modify wrong and omitted words	02/09/2003
2.30	・Add a new model to the type of MJX ・Add a setting screen of MJXDEBW ・Add a setting screen of ETM	20/02/2004

Notes

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Printed in Japan

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February 2004

This manual is composed of the following contents:

Chapter 1. Configuration File
This chapter describes the explanation of configuration file and the information to set it .

Chapter 2. Selecting MJX Model
This chapter describes how to select the type of MJX Model.

Chapter 3. Selecting CPU
This chapter describes how to select the type of CPU.

Chapter 4. Setting Configuration
This chapter describes how to set configuration as follows.

Contents

Chapter 1. Configuration File

The environmental setting, which is necessary to start MJXDEBW debug program, is described in Configuration file.

Before starting MJXDEBW debug program, you must prepare a configuration file that fit to your target system.

Support program of Configuration setting (MjxCfg.exe) is used to set a configuration.

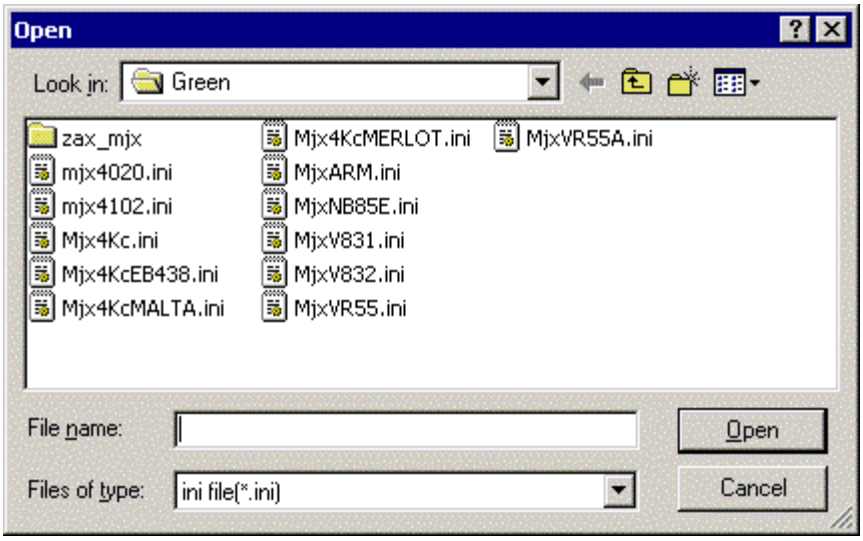
【Note】 Please set a configuration carefully. IF the setting is failed, MJXDEBW debug program may not work normally

Please don’t rewrite a Configuration file (a text file) except Configuration setting support program.

Procedure to start Configuration Support program (MjxCfg.exe) is described.

After turning on the power of all peripheral equipment, please start MJXCFG from start menu.
Procedure is as follows

1. start menu
2. program(P)
3. MJX440 Tools
4. MJXCFG Configuration Tool



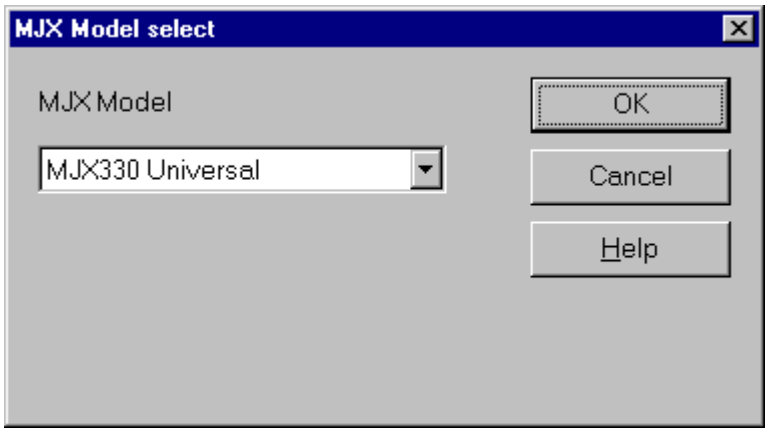
Please use a template for each type of CPU which you use.
When you prepare a new configuration, please specify it.

The setting of configuration is classified as follows.

Chapter 2. Selecting MJX Model

Selecting the type of MJX Model

It is possible to select a type of MJX Model only when a new Configuration file is prepared.

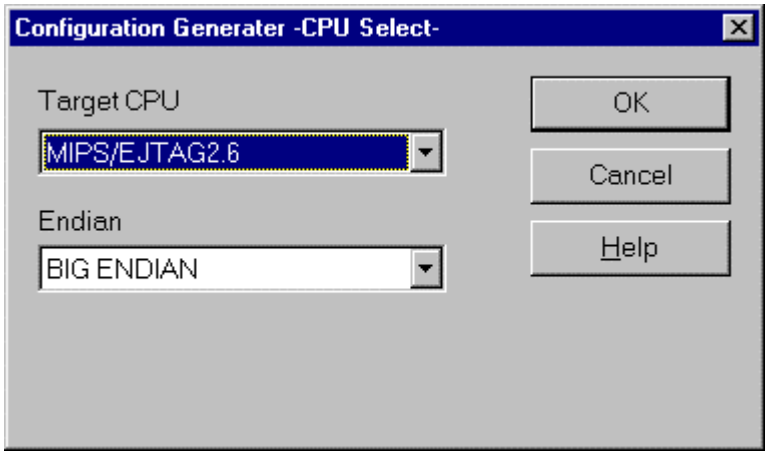


【Note】 In case of 「MJX330 for ARM7/9」, the product, whose model number which is described on the back side of MJX330 main body is **MJX330-ARM-XXX,** is the old model of 「MJX330 for ARM7/9」.
In this case, please select 「MJX330 for ARM7/9」.
In other cases, please select 「MJX330 Universal」 and 「ARM7/9」 in 「Chapter 3 Selecting CPU」.

Chapter 3. Selecting CPU

Selecting the type of CPU

It is possible to select a type of CPU only when a new Configuration file is prepared.
It is impossible to alter a type of CPU of existing Configuration files.
Required fields in Configuration Generator dialog are different at each CPU.
When target CPU is Bi-endian, you must specify endian.
It is impossible to change endian setting while program is running..



【Note】 In case you select a individual model (except「MJX330 Universal」) in「Chapter 2 Selecting MJX Model」, this window may not appear.
In this case, please go to「Chapter 4 Setting Configuration」.

Chapter 4. Setting Configuration

This chapter describes how to set configuration and is classified as follows.
The configuration setting is different from each model.
Please set with below links.

●MJX330 for ARM7/9
- Setting MJX330
- Setting JTAG
- Setting ENV
- Setting MJXDEBW
- Setting FLASH
- Setting MJX330 for ARM

●MJX330 for EJtag2.5/2.6
- Setting MJX330
- Setting JTAG
- Setting ENV
- Setting MJXDEBW
- Setting FLASH
- Setting MIPS/Ejtag2.6

●MJX330 for VR5500
- Setting MJX330
- Setting JTAG
- Setting ENV
- Setting MJXDEBW
- Setting FLASH
- Setting VR5500

●MJX330 for NB85E
- Setting MJX440
- Setting ROM
- Setting ENV
- Setting NB85E

●MJX440 for V831/832

Setting MJX440
Setting ROM
Setting ENV
Setting V831

●MJX440 for NB85E

Setting MJX440
Setting ROM
Setting ENV
Setting NB85E

●MJX440 for TR4102/CW4020

Setting MJX440
Setting ROM
Setting ENV
Settng FLASH
Setting MIPS/EJtag

●MJX440 for ARM7/9

Setting MJX440
Setting ROM
Setting ENV
Setting ETM
Setting MJX440 for ARM

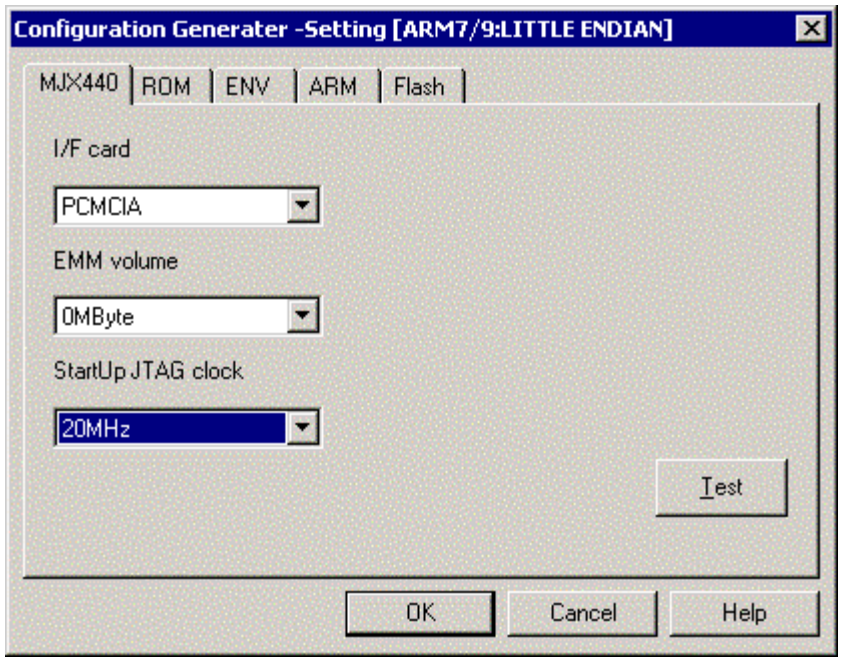
【Note】 In case of「MJX330 for ARM7/9」, the product ,whose model number ,which is described on the back side of MJX330 main body , is **MJX330-ARM-XXX,** is the old model of「MJX330 for ARM7/9」.
In this case, please set the same setting with「MJX330 for ARM7/9」in Configuration Setting.

4.1 Setting each product

4.1.1 Setting MJX440（MJX440）

This clause describes the setup of MJX440 main body.

【Note】In case you purchase general-purpose products of「MJX330 for MIPS/EJTAG2.6」,「MJX330 for VR5500」 and「MJX330 for ARM」, there is no setting for MJX440.Please refer to「4.1.2 MJX330 Setting」.



StartUp JTAG clock

Clock frequency is specified when MJX440 is started up.
Clock frequency, which can be set, is different from each MJX440 model.
JTAG clock frequency is altered by a command of MJXDEBW.
The higher the clock frequency is, the faster access speed of a target board is.
If target board cannot be accessed at the specified frequency, please specify lower frequency.

I/F Card

The classification for Host Interface is specified.
Please select one of PCI/PCMCIA/USB/LAN.

【Note】When host computer have both PCI and PCMCIA interface, the interface which is selected above field can be selected.

EMM Volume

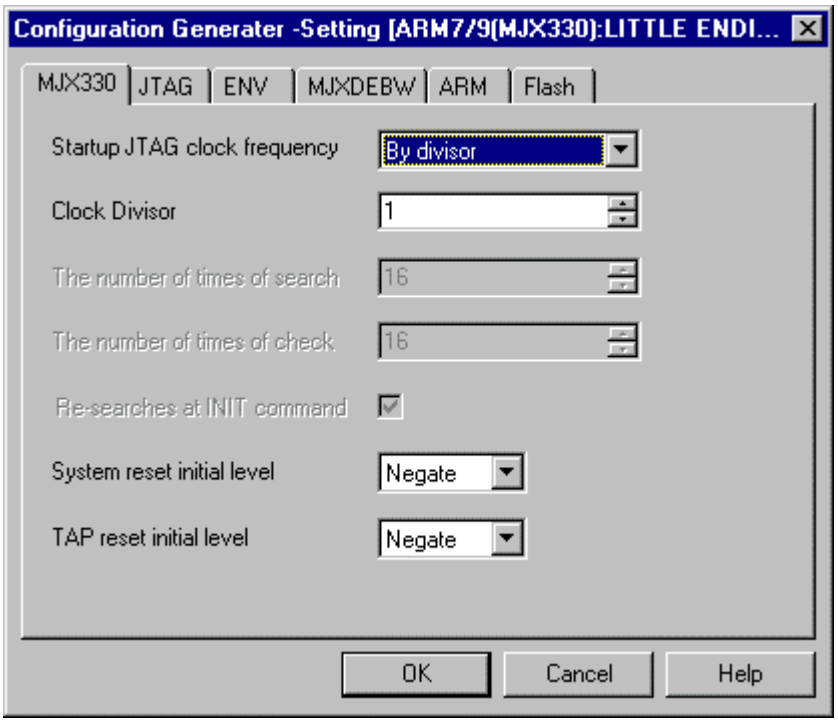
The volume of Emulation Memory mounted on MJX440 is specified.
Please select one of 0Mbyte/4Mbyte/8Mbyte/16Mbyte.

【Note】If you purchased products「MJX330 for NB85E」, please refer to Setting MJX440.
In this case, please be sure to set PCMCIA in I/F Card field and 0Mbyte in EMM Volume field.
Besides 25MHz/12.5MHz is displayed in StartUp JTAG clock field when「MJX330 for NB85E」is used, Real JTAG Clock is 20MHz/10MHz.

4.1.2 Setting MJX330（MJX330）

This clause describes　the setup about MJX330 main body.

【Note】 The general-purpose products of「MJX330 for MIPS/EJTAG2.6」,「MJX330 for VR5500」and「MJX330 for ARM」 model need a setting for MJX330.
Other models don't need this setting.



Startup JTAG clock frequency

Specify the way to determine JTAG clock frequency in starting MJXDEBW.
Please select the one of followings.

By divisor
Set the division ratio against MJX330 system clock

Automatic optional search
Search the movable JTAG clock frequency automatically.

RTCK synchronization （only ARM9E-S core）
Perform RTCK synchronous behavior

When you select「By divisor」, you need to specify「Clock Divisor」.

When you select「Automatic optional search」, you need to specify「The number of times of search」, 「The number of times of check」 and「Re-searches at INIT command」.
When you select「RTCK synchronization」, there is no additional items to specify.

【Note】It is possible to set only「By divisor」item for general purpose products of「MJX330 for MIPS/EJTAG2.6」and「MJX330 for VR5500」.

Clock Divisor
JTAG Clock frequency when MJX330 starts is specified by division ratio against system clock.
Division ratio can be specified between 1 and 4096
System clock of usual product is 40MHz.

The number of times of search
Input the number of times of automatic search.
When you specify a large number, you can search the maximum clock in higher accuracy, but starting time become longer.

The number of times of check
Input the number of times to confirm whether it works certainly with trial frequency in automatic searching.
Error may occur when the number is too small because it mistakes the judgment whether it can work or not.

Re-searches at INIT command
In executing init command or selecting「Emulation」－>「initialize」from menu, it specify whether it perform the JTAG clock automatic optional search or not

System reset initial level
Input the initial value of JTAG system reset signal.
The specified value is set when MJXDEBW is exited.

TAP reset initial level
Input initial value of JTAG TAP reset signal.
The specified value is set when MJXDEBW is exited.

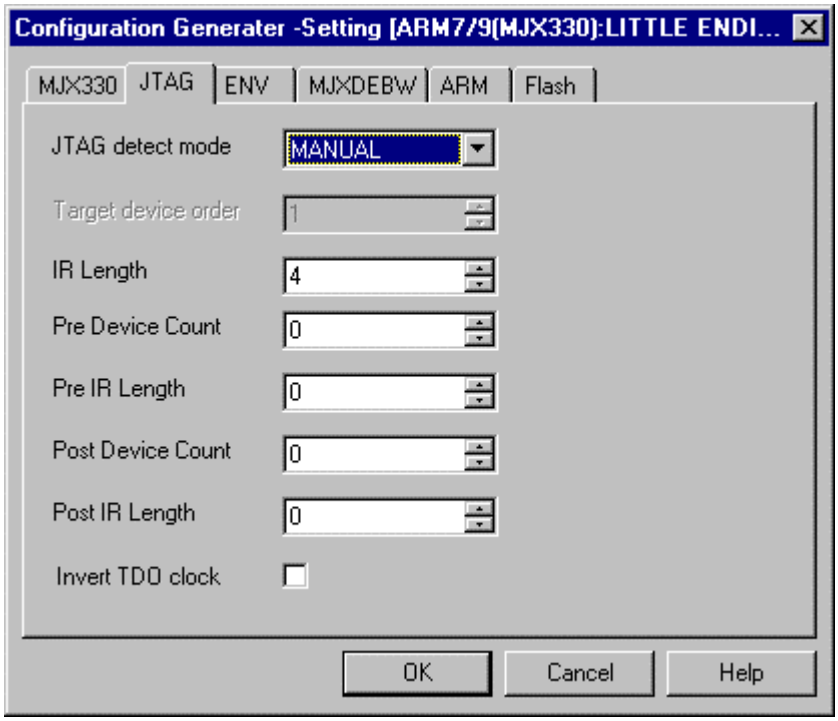
【Note】If you purchased products「MJX330 for NB85E」, please refer to「4.1.1 Setting MJX440」.

【Note】 Nonvolatile memory isn’t mounted on MJX330 main body.
So JTAG signal, like system reset or so, is set not to a specified initial value but to “negate” just after power-up of PC.
To set the specified initial value, please start and exit MJXDEBW.

4.2 Setting JTAG(JTAG)

This chapter describes the setup about JTAG.

【Note】 General purpose product of「MJX330 for MIPS/EJTAG2.6」,「MJX330 for VR5500」 and「MJX330 for ARM」 need to set JTAG.
Other models don't need this setting.



JTAG detect mode

Select a detection mode.

AUTO

Measure the number of device, which is connected by JTAG chain, and each IR length.
Specify the target CPU for debug by specifying the order of a target device only.

MANUAL

Specify the target CPU for debug with IR length／Pre Device Count･Post Device Count･IR Length.

Target device order

Specify the order of target CPU for debug in JTAG chain.

IR

You input the bit width of JTAG Instruction register (IR) of the target CPU.

Pre Device Count

When some devices are connected by JTAG chain, you input the total number of devices which are connected in front of the target CPU for debug. (TDI side)

Pre IR Length

When some devices are connected by JTAG chain, you input the total number of IR length of each device which are connected in front of the target CPU for debug.

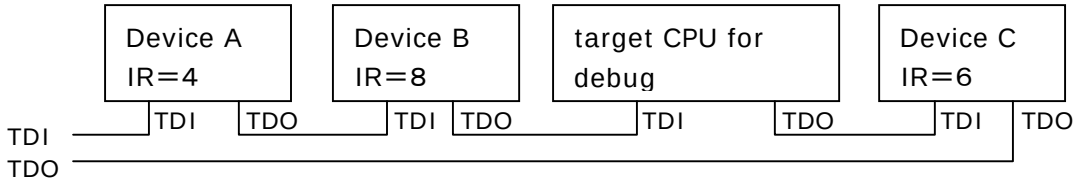
Post Device Count

When some devices are connected by JTAG chain, you input the total number of devices which are connected at the back of the target CPU for debug.

Post IR Length

When some devices are connected by JTAG chain, you input the total number of IR length of each device which are connected at the back of the target CPU for debug.

Example



The order of target device	3	(the order which count from TDI side)
IR	5	(IR length of the target CPU for debug)
Pre Device count	2	(Device A and Device B)
Pre IR Length	12	(IR length of Device A＋IR length of Device B)
Post Device count	1	(Device C)
Post IR Length	6	(IR length of Device C)

Invert TDO Clock

Sampling Edge of TDO can be changed from rising edge to falling edge of JTAG standard clock.

Additional

Guideline in case TDO is delayed when high frequency of JTAG Clock is used.

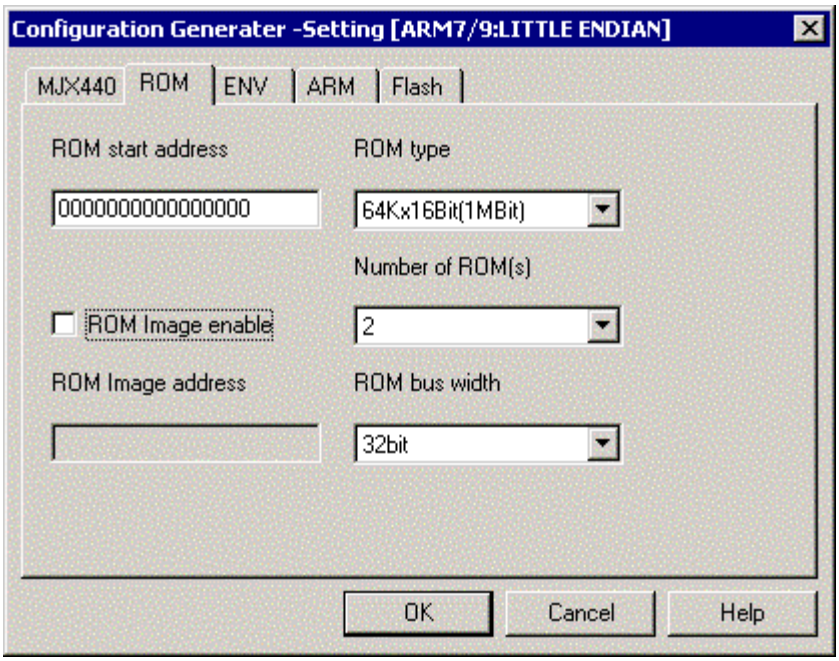
When high frequency of JTATG clock is used, TDO cannot be sampled with JTAG standard clock because of TDO delay time affected by cable. And Error may cause.

In this case, please adjust the timing of TDO sampling by setting following parameters.

	invert TDO clock	Post Device Count	remark
high ↓ low	inversion	+0	
	non-inversion	+0	standard
	inversion	+1	
	non-inversion	+1	

4.3 Setting Emulation Memory（ROM）

This chapter describes how to set Emulation Memory



ROM start address

Start address of ROM area on target board is specified with logic address(hexadecimal number).
When some ROM's are mounted on target board , please specify the start address of the ROM which is mapped in the last address.
Please specify the start address of the ROM.
(Example) When two ROM's, one start with address 0x00100000 and the other start with 0x00180000, are mounted on the target system, you specify 0x00100000.

ROM Image enable

The target system, which don't decode address fully and CPU which different logic address
Target system, which isn't decoded completely, or CPU ,in which different logic address access to same physical address, may have ROM image area which can be accessed as ROM area.
To set this area to emulation memory, set to「enable」.

ROM Image address

specify the start address of ROM Image Area by hexadecimal number.

ROM bus width

Specify the ROM bus width
The data bus width is specified when the ROM of target system is read.
Please one of 8/16/32/64.
Please be sure in case this bus size is different from the one of CPU.

ROM type

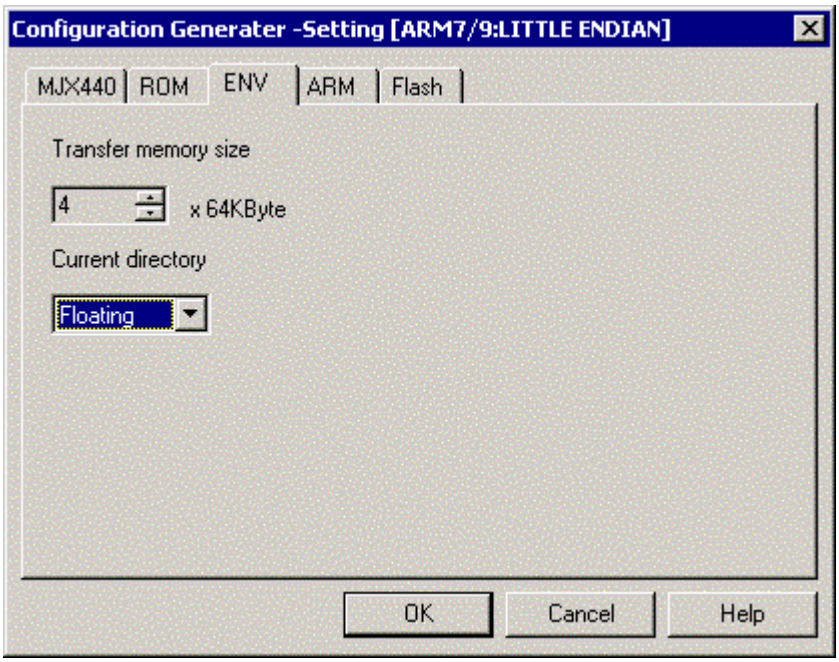
Specify the type of ROM which is used for target system.
Please select one of
64Kx16Bit(1MBit)/128Kx8Bit(1MBit)/128Kx16Bit(2MBit)/256Kx8Bit(2MBit)/
256Kx16Bit(4MBit)/512Kx8Bit(4MBit)/512Kx16Bit(8MBit)/1Mx8Bit(8MBit)/
1Mx16Bit(16MBit)/2Mx8Bit(16MBit)/2Mx16Bit(32MBit)/4Mx8Bit(32MBit)/
4Mx16Bit(64MBit).

Number of ROM(s)

Specify the number of ROM(s) which are used for Emulation.
Please select one of 0/1/2/4/8 .

4.4 Environment of Host Computer(ENV)

This chapter describes the setup about Host Computer.



Transfer memory size

Specify the size of Transferred buffered memory which is used for MJXDEBW debugger program with every 64Kbyte.

Debugger Program have hierarchical structure, in fact, four times as large as buffered memory are necessary.

Swap may occur when large size of memory is set, and the speed of transferring may become low.

We can't except the good change even if large size is set.

【Note】When USB or LAN is used as Host Interface , please don't set the size of Transferred buffered memory to over 512Kbyte.

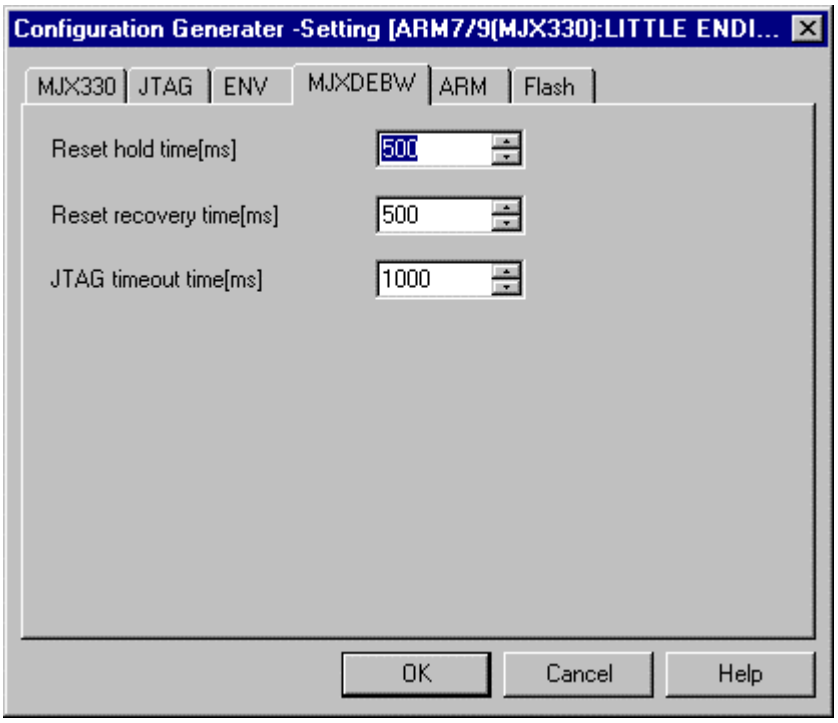
Current directory

When Download is executed while using MJXDEBW debugger program,「Open file」dialog appears.
In case「Floating」is set , directory is moved to which is selected in current directory.
In case「Fixed」is set , directory isn't moved.

【Note】In starting MJXDEBW debugger program, dialog box appears to select configuration file.In this time, current directory is moved Irrespective of configuration setting. That is to say, the current directory in starting MJXDEBW debugger program is the one which configuration exist.

4.5 Setting MJXDEBW(MJXDEBW)

This chapter describes the setup about MJXDEBW debugger program.



Reset Hold Time[ms]

Input the time of JTAG system reset signal that MJXDEBW program hold in resetting target.

Reset recovery time[ms]

Input the wait time that the operation of debugger start after resetting.

JTAG timeout time[ms]

Input the time to judge timeout error when JTAG is working.

【Note】 General purpose product of 「MJX330 for MIPS/EJTAG2.6」 and 「MJX330 for VR5500」model can be set only 「Reset hold time[ms]」.

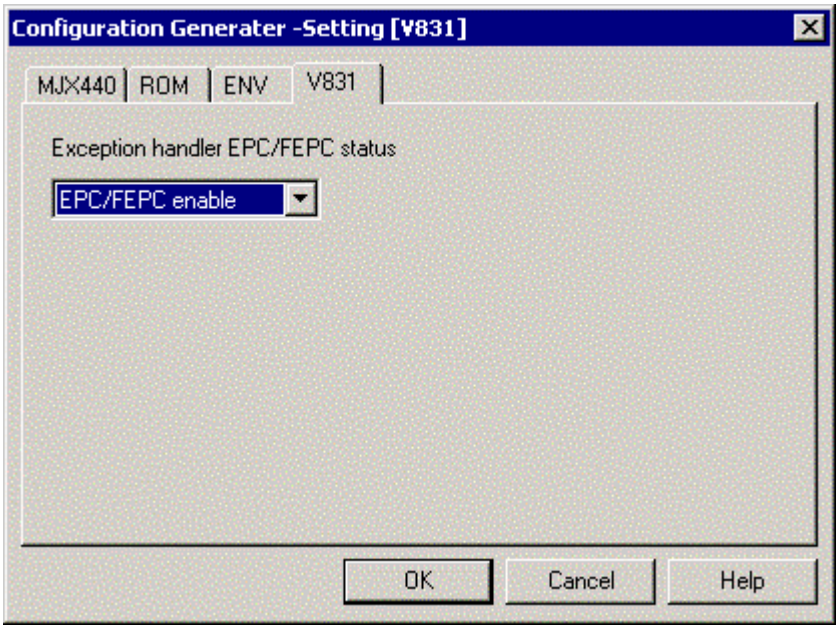
4.6 Setting each type of CPU

The setup for each CPU have its own way.

Please set a CPU type followed by the one you use.

4.6.1 Setting V831（V831）

This clause specifies the particular setup for V831.



Select Exception handler EPC/FEPC Enable/Disable

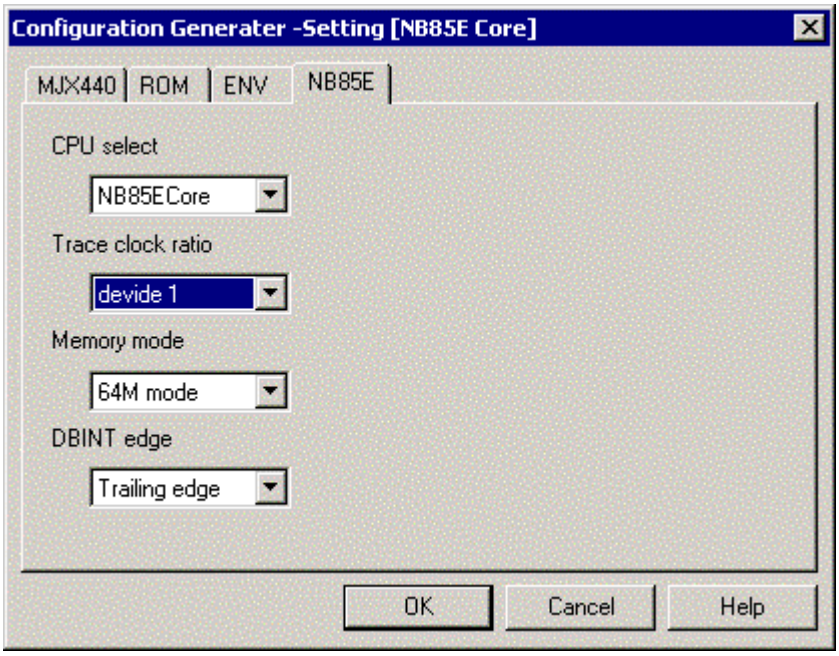
Exception handler stops in Exceptional Handler.

Setting up whether EPC/FEPC is used as exception (Interrupt) address or not, in case a disassembler display of Trace is done.

In rewriting EPC/FEPC in Exceptional Handler or using RTOS, please set to「disable”.

4.6.2 Setting NB85E(NB85E)

This clause specifies the particular setup for NB85E.



CPU select

Select the type of CPU with the followings.

- ・NB85ECore
- ・V850E/ME2

Trace clock ratio

The frequency of N-Wire trace clock can be changed to one or two dividing of VBCLK frequency in using NB85ECPU core.

Please be sure not to set the value more than maximum clock frequency of MJX440 for NB85E (66MHz).

Memory mode

Specify the memory mode which is used for target CPU core.

Please select one of 64M mode and 256M mode.

DBINT edge

This item can be used when you want to stop a program compulsorily by External input signal. (External trigger brake function)

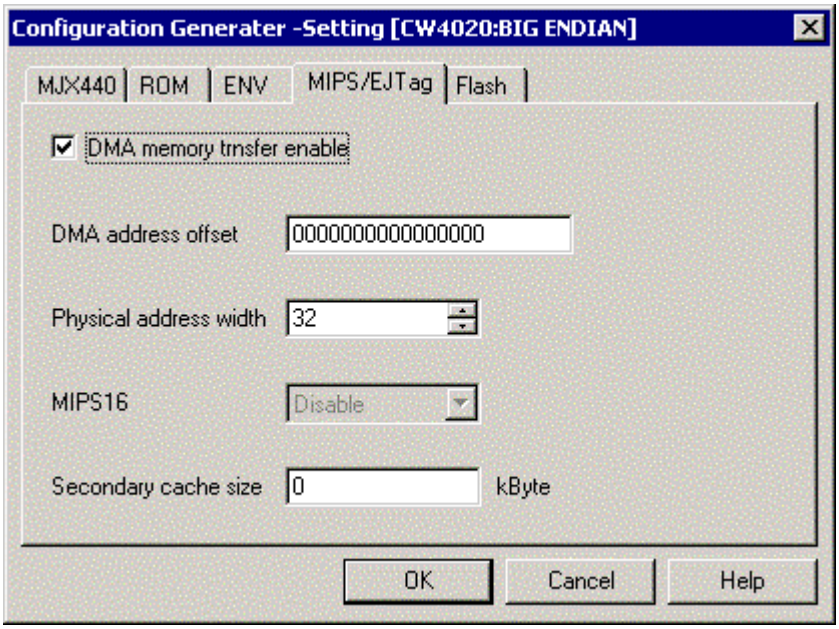
Select the one of 「invalid」/「trailing edge」/「falling edge」

In case external trigger brake function isn't used, please set 「invalid」.

In case external trigger brake function is used, please specify the edge.

4.6.3 Setting MIPS/EJTAG(MIPS/EJTAG)

This clause specifies the particular setup for TR4102/CW4020.



DMA memory transfer enable

This item decide whether you use DMA function of CPU or not, in accessing to memory on target board.

When you set this item valid, memory can be accessed rapidly. Download speed of object file become rapid.

【Note】DMA transfer can be used only when EJTAG of CPU have DMA function.
The area of physical address in memory is written directly by DMA transfer.
So. DMA transfer can be used when the mapping of logic address and physical address are not obvious and logic address is mapped to discontinuous physical address by virtual Operating System.

DMA address offset

DMA transfer can write to a area of the physical address directly.

This item is specified when Logic address and physical address have offset.

CPU Physical address width

This item can specify the physical address width of CPU between 32bit and 64bit

【Note】 In case of MJX440 for TR4102/CW4020, you cannot specify except 32 and 64.

MIPS16

This item can specify whether you use MIPS16 instruction or not.

【Note】 In current version , you cannot use MIPS16 instruction.

Secondary cache size

This item can specify the size of secondary cache every 64 kByte

If secondary cache doesn't exist , please set to "0".

＜supplementary information＞
DMA address offset

MJX440 can access to target resource(memory) by the following ways.

・DMA - execute by using DMA* function of DSU(Debug Support Unit) in CPU.

・monitor - execute the program which is operated by kernel mode of CPU.

DMA operate rapidly because it is the function of PCU hardware.
Monitor operate fairly slowly because it is executed with JTAG cable.
You can use DMA, when a trouble occurs on target board, and CPU, which don't have DMA function.
You can specify the function (DMA or monitor) with MJXCfg.exe, which is the configuration support tool
If CPU have the DMA function,「DMA memory transfer enable 」and「DMA address offset」are valid.
(If CPU don't have the DMA function,「DMA memory transfer enable 」and「DMA address offset」are invalid)。
When DMA function can be used, you need to check「DMA memory transfer enable」on.
And please specify「DMA address offset」.
Following explain the meaning of「DMA address offset」.
Software (OS and Application) working on CPU use Virtual address, OS (Operation System), which realize Virtual memory using TLB (Translation Lookaside Buffer) of MMU (Memory Management Unit) in CPU , convert it to physical address corresponding to real memory.
DMA function use physical address in accessing to target resource (memory) because it is hardware function in CPU.
When you use DMA function, it is necessary for MJXDEBW debugger to execute address translation from Virtual address to Physical address, instead of MMU, because address translation of MMU/TLB cannot be used.

MJXDEBW debugger process this address translation as additional expression.

Physical address = Virtual address ＋ DMA address offset

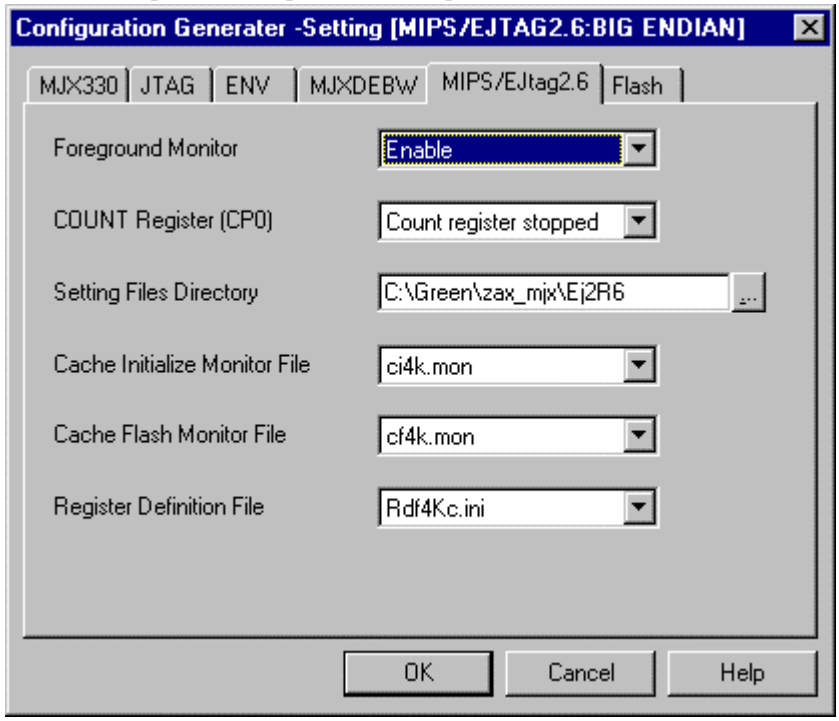
For example, when file data have data beginning with virtual address 1000h , if that data is downloaded to the physical address beginning with 8000h, you need to set「DMA address offset」to 7000h which is the difference between 8000h and 1000h.
Address translation is the following.

Physical address = Virtual address ＋ 7000h

*1 DMA = Direct Memory Access

4.6.4 Setting MIPS/EJTAG2.6 (MIPS/EJTAG2.6)

This clause specifies the particular setup for MIPS/EJTAG2.6.



Foreground Monitor

When it is possible to execute downloading rapidly by using the parts of target memory as monitor area, when you download MJX binary type of object file with Mjxdebw program.

Please set「Foreground Monitor」 to「Enable」.

It is possible to execute downloading more rapidly with Rapid download function of EJTAG which is the function after EJTAG2.6.

Please set「Foreground Monitor」 to「Enable(fast)」.

【Note】

1. If program cannot be executed in memory area which is downloaded, download can not be executed normally with「Enable」 or「Enable(Rapid)」.
2. If you set「Foreground Monitor」 to「Enable」, detection of exception for memory access(TLB exception) is not executed. If it is clear not to occur a exception, please set this field to the area only when it is clear not to occur .
3. EJTAG2.5 can't set「Enable（Rapid）」.

COUNT Register(CP0)

When a application program on a target board stop and is in debug mode, the count of COUNT Register of CP0 is set to continue or stop.

【Note】Target CPU may not have the above function. Please refer to the manual of target CPU you use about details.

Setting Files Directory[*1]

This field specify the directory which save files of「Cache Initialize Monitor File」、「Cache Flash Monitor File」and「Register Definition File」.
Please specify the directory with「…」button.

【Note】If you set「Environment of Host Computer(ENV)」field to「Floating」,please be sure to set this field with absolute path. Sometimes, INIT command don't act with normal.

Cache Initialize Monitor File

This field specifies a file in which a program is described to initialize the cache of CPU for debug.

Cache Flash Monitor File

This field specifies a file in which a program is described to flash the cache memory for debug.

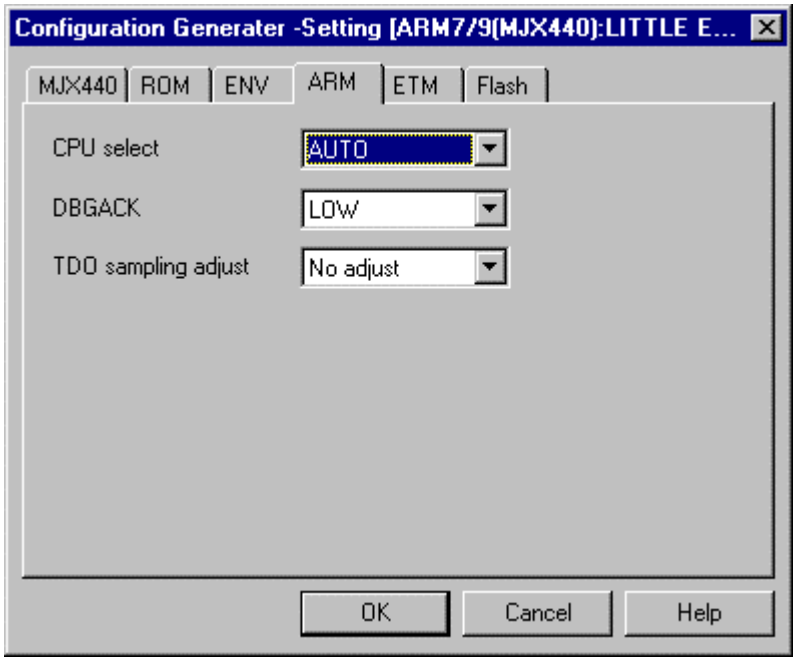
Register Definition File

This field specifies the Register Definition File which describes register configuration of CPU to debug.

[*1] A file which is in a directory specified in「Setting File Directory」is alternatives of「Cache Initialize Monitor File」,「Cache Flash Monitor File」and「Register Definition File」.

4.6.5 Setting ARM(ARM) /MJX440 for ARM

This clause specifies the particular setup for MJX440 for ARM.



CPU Select

Select a CPU model

DBGACK

This field specify each of「LOW」and「HIGH」.

This setting reflects to DBGACK which is output signal of ARM core, when memory access is done by debugger, and 0th bit of Debug control register of Embedded ICE in debug mode.

Please refer to the manual of target CPU you use about details.

TDO sampling adjust

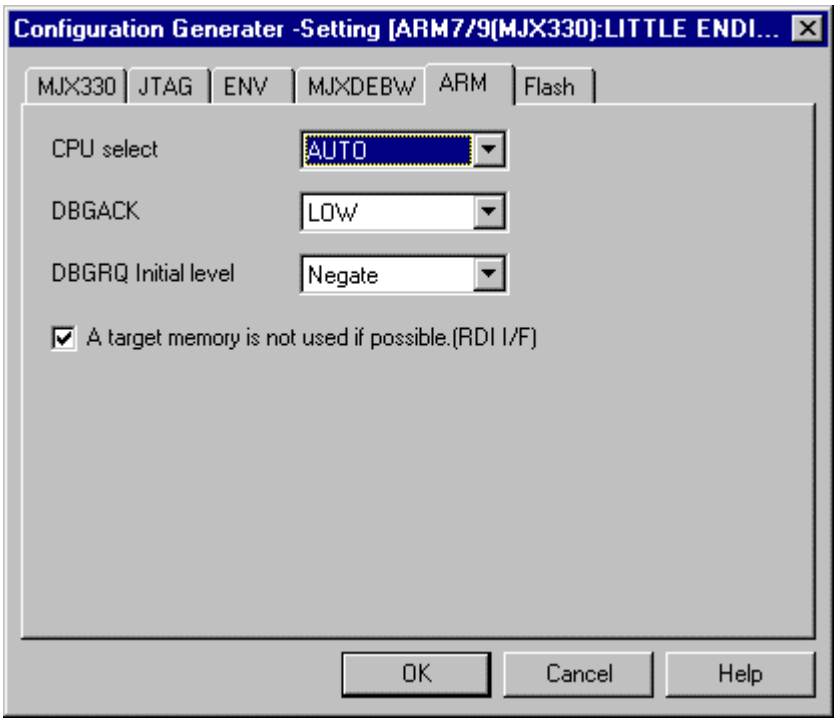
Adjustment of TDO sampling can be set with「+1 TCK」or「No adjust」.

Timing adjustment of JTAG interface circuitry is done. Please select「No adjust」, ordinarily.

When TCK is more than or equal to 40 MHz and the latency of the TDO output from TCK falling edge is more than or equal to 10ns, please select「+1 TCK」.

4.6.6 Setting ARM(ARM) /MJX330 for ARM

This clause specifies the particular setup for MJX330 for ARM of general purpose product.



CPU Select

Select a CPU model

DBGACK

This field specify one of「LOW」and「HIGH」.

This setting reflects to DBGACK which is output signal of ARM core, when memory access is done by debugger, and 0^{th} bit of Debug control register of Embedded ICE in debug mode.

Please refer to the manual of target CPU you use about details.

DBGRQ Initial level

Input the initial value of JTAG DBGRQ signal.

It is set to specified value when MJXDEBW is exited.

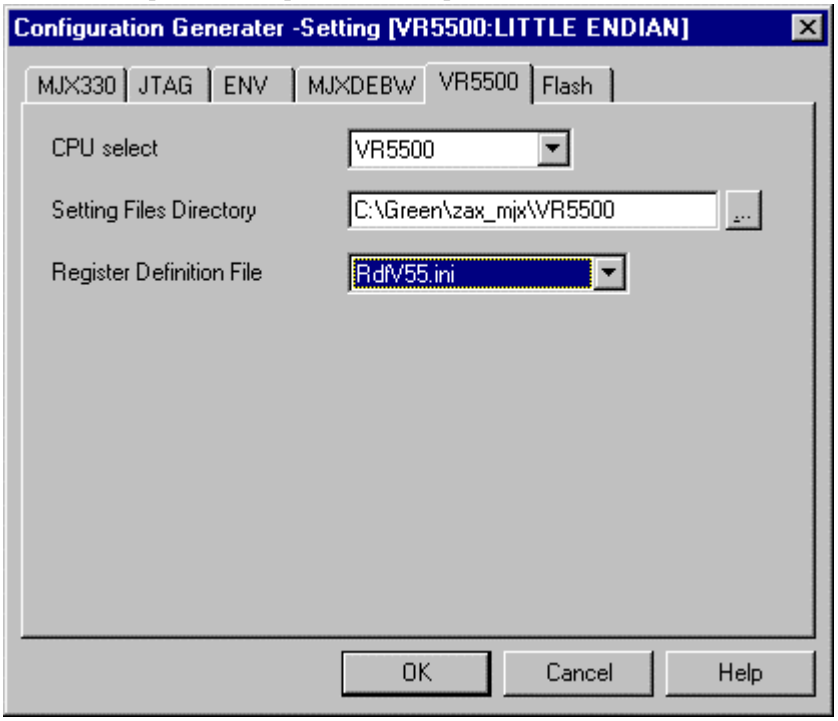
A target memory is not used if possible.[RDI I/F]

Target execution instructions of RDI I/F, like MCR/MRC instruction to CP15, is switched to JTAG scan, and a target memory is not used.

【Note】 In case of using RDI I/F, even if you don’t use the function of writing to flash memory, please set 「Setting Flash」－「RAM work area top address」.

4.6.7 Setting VR5500(VR5500)

This clause specifies the particular setup for VR5500.



CPU select

select CPU model.

Setting File Directory

This field specify the directory which save「Register Definition File」.
Please specify the directory with pushing「…」button.

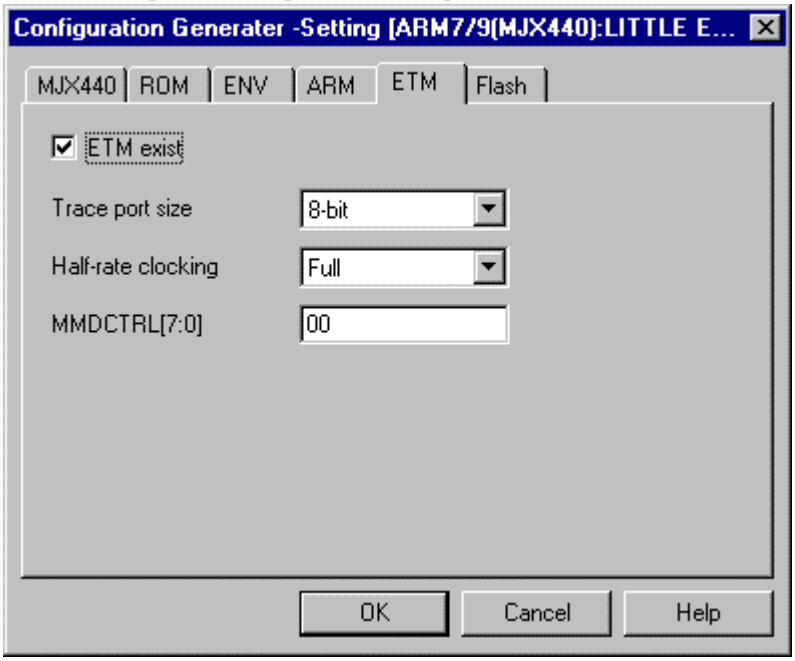
【Note】When you set「Current directory」field of Environment of Host Computer(ENV) to「floating」, please be sure to set this with absolutory path. Sometimes, INIT command operate normally.

Register Definition File

This field set the register definition file which is described about register configuration of target CPU for debug.

4.7 Setting ETM(ETM)

This clause specifies the particular setup for ETM.



ETM exist

If target CPU have ETM function, please check this field.
If this field is checked, you can display Trace after executing user program.

Trace port size

This field set the size of Trace port to each value of 4, 8 and 16-bit.
Maximum port size you can use is different from the package of target CPU.
Please refer to the manual of target CPU you use about details.

Half-rate clocking

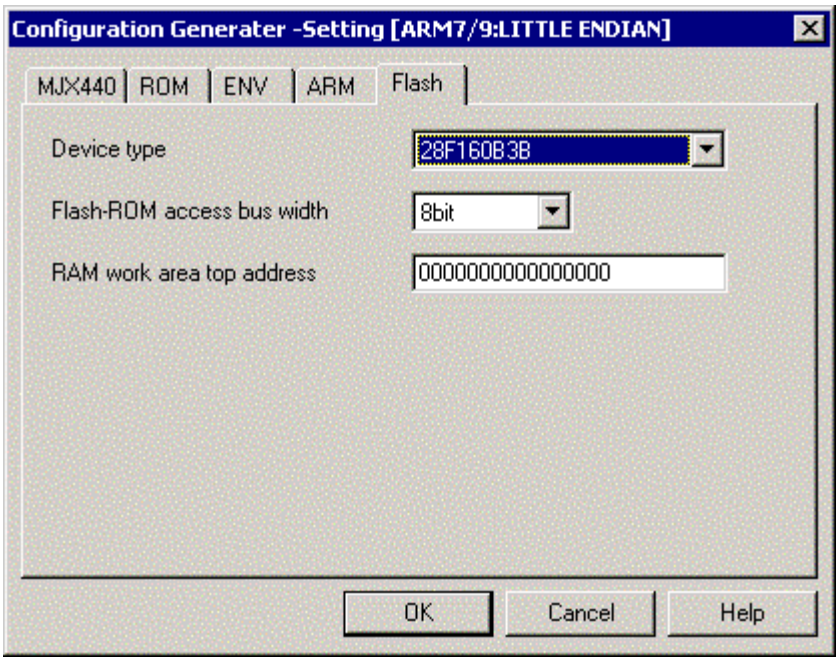
You can set to「Half」or「Full」.
「Full」may not be set because of packaging of target CPU.
Please refer to the manual of target CPU you use about details.

MMDCTRL [7:0]

This field specify the data which is written to Memory map decode control register between 0x0000 to 0x00FF.

4.8 Setting Flash（Flash）

This clause specifies the particular setup for flash memory.



Device type

This field specify the device name of flash memory.
You need Device information definition file of each type of flash memory.
Please refer to MJX440 User's Manual about details.

Flash-ROM access bus width

This field set the data bus width when Flash-Rom is accessed on target system.
Please select the one of 8/16/32/64.
Be careful of the case when data bus width is different from the one of CPU.

RAM work area top address

This function, which write to flash memory, use the Ram area of target system.
Please input the address which is usable for ram area.
Ram capacity which is necessary to write to flash memory is calculated by following equation.

18KByte＋(All sector number of flash device×8)Byte＋updated sector size※1

【Note】Device type and access bus width of Flash-ROM are established value of FLASH command.
You can write with bus width which is different from a value set by configuration file , if you specify it explicitly.

※1 select the largest size in case some size exist.

Reference words