TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

524,288-WORD×2 BANK×16-BIT SYNCHRONOUS DYNAMIC RAM

DESCRIPTION

The TC59S1616AFT is CMOS synchronous dynamic random access memory devices, organized as 524, 288 words×2 banks×16 bits, respectively. Fully synchronous operations are referenced to the leading edge of the clock input and can transfer data at up to 125M words per second. These devices are controlled by command settings. Each bank is kept active so that the DRAM core sense amplifiers can be used as a cache. The refresh functions, Auto Refresh and Self-Refresh, are easy to use. Using the programmable Mode register, the system can choose the mode which will maximize its performance. These devices are ideal for main memory in applications such as workstations.

FEATURES

ITEM		TC59S1616			
		-8	-10	-12A	-12
t_{CK}	Clock Cycle Time (min)	8 ns	10 ns	12 ns	12 ns
t_{RAS}	Active to Precharge Command Period (min)	48 ns	60 ns	60 ns	72 ns
t_{CAC}	Access Time from Read Command (max)	23.5 ns	24 ns	24 ns	27.5 ns
t_{AC}	Access Time from CLK (max) ($\overline{CAS}$ Latency = 3)	7.5 ns	8.5 ns	9 ns	9 ns
t_{RC}	Ref/Active to Ref/Active Command Period (min)	80 ns	100 ns	100 ns	120 ns
I_{CC1}	Operation Current (max) (Single Bank)	110 mA	90 mA	90 mA	80 mA
I_{CC6}	Self-Refresh Current (max)	2 mA	2 mA	2 mA	2 mA

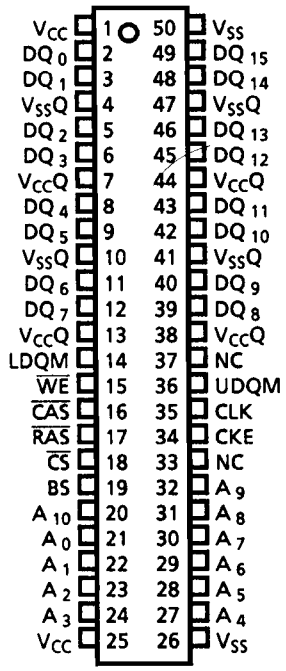
- Single power supply of 3.3 V±0.3 V
- Up to 125 MHz clock frequency
- Synchronous operations: All signals referenced to the positive edges of the clock
- Architecture: Pipeline
- Organization
  TC59S1616AFT : 524, 288 words×2 banks×16 bits
- Programmable Mode register
- Auto Refresh and Self Refresh
- Burst Length : 1, 2, 4, 8, Full page
- $\overline{CAS}$ Latency : 1, 2, 3
- Single Write mode
- Burst Stop function
- Byte data controlled by L-DQM, U-DQM
- 4K Refresh cycles / 64 ms
- Interface: LVTTL
- Package
  TC59S1616AFT : TSOP II 50-P-400-0.80B (Weight : 0.51g typ.)

PIN NAMES

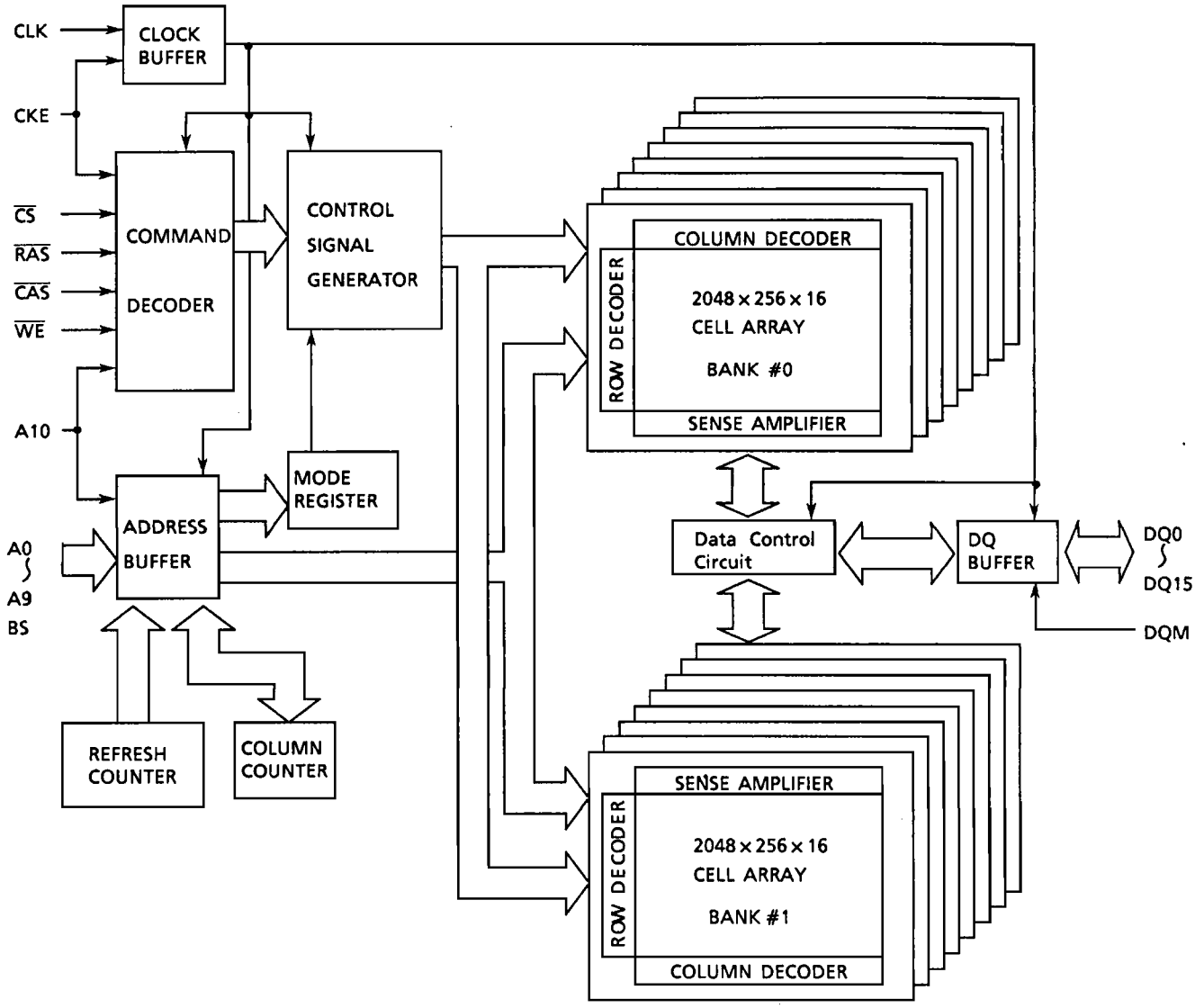
A0 to A10	Address
BS	Bank Select
DQ0 to DQ15 (TC59S1616)	Data Input / Output
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
UDQM/LDQM (TC59S1616)	Output Disable / Write Mask
CLK	Clock inputs
CKE	Clock enable
V_{CC}	Power (+3.3V)
V_{SS}	Ground
$V_{CC}Q$	Power (+3.3V) (for I/O buffer)
$V_{SS}Q$	Ground (for I/O buffer)
NC	No Connection

PIN ASSIGNMENT (TOP VIEW)

TC59S1616AFT



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTES
V_{IN}, V_{OUT}	Input, Output Voltage	−0.3 to V_{CC} + 0.3	V	1
V_{CC}, $V_{CC}Q$	Power Supply Voltage	−0.3 to 4.6	V	1
T_{OPR}	Operating Temperature	0 to 70	°C	1
T_{STG}	Storage Temperature	−55 to 150	°C	1
T_{SOLDER}	Soldering Temperature (10s)	260	°C	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V	2
$V_{CC}Q$	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	2.0	−	V_{CC} + 0.3	V	2
V_{IL}	Input Low Voltage	- 0.3	−	0.8	V	2

NOTE: V_{IH} (max) = V_{CC} / $V_{CC}Q$ + 1.2V for pulse width ≦ 5ns
V_{IL} (min) = V_{SS} / $V_{SS}Q$ − 1.2V for pulse width ≦ 5ns

CAPACITANCE (V_{CC} = 3.3V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS
C_I	Input Capacitance (A0 to A10, BS, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, LDQM, UDQM, CKE)	−	4	pF
	Input Capacitance (CLK)	−	6	pF
C_O	Input / Output Capacitance	−	5	pF

NOTE: These parameters are periodically sampled and not tested for every component individually.

RECOMMENDED DC OPERATING CONDITIONS (V_{CC} = 3.3V ± 0.3V, Ta = 0° to 70°C)

ITEM		SYMBOL	MAX(×16)				UNITS	NOTES
			-8	-10	-12A	-12		
OPERATING CURRENT t_{CK} = min, t_{RC} = min Active Precharge command cycling without Burst operation	1-bank operation	$I_{CC}1$	110	90	90	80	mA	3
	2-bank interleave operation	$I_{CC}1B$	150	130	130	115		3
STANDBY CURRENT t_{CK} = min, $\overline{CS}$ = V_{IH} $V_{IH/L}$ = V_{IH}(min) / V_{IL}(max) Bank : inactive state	CKE = V_{IH}	$I_{CC}2$	35	30	28	28		3
	CKE = V_{IL} (Power Down mode)	$I_{CC}2P$	2	2	2	2		
STANDBY CURRENT CLK = V_{IL} , $\overline{CS}$ = V_{IH} input signals are stable. $V_{IH/L}$ = V_{IH}(min) / V_{IL}(max) Bank : inactive state	CKE = V_{IH}	$I_{CC}2S$	13	13	13	13		
	CKE = V_{IL} (Power Down mode)	$I_{CC}2PS$	2	2	2	2		
NO OPERATING CURRENT t_{CK} = min $\overline{CS}$ = V_{IH}(min) Bank : active state (2 banks)	CKE = V_{IH}	$I_{CC}3$	85	75	70	70		3
	CKE = V_{IL} (Power Down mode)	$I_{CC}3P$	3	3	3	3		
BURST OPERATING CURRENT t_{CK} = min Iout = 0mA Bank : active state (2 banks)	Read Cycle	$I_{CC}4R$	155	135	125	125		3, 4
	Write Cycle	$I_{CC}4W$	150	125	115	115		3
AUTO REFRESH CURRENT t_{CK} = min , t_{RC} = min Auto Refresh command cycling		$I_{CC}5$	80	65	65	60		3
SELF REFRESH CURRENT CKE = 0.2V Self Refresh mode		$I_{CC}6$	2	2	2	2		

ITEM	SYMBOL	MIN	MAX	UNITS	NOTES
INPUT LEAKAGE CURRENT (0V ≦ V_{IN} ≦ V_{CC}, all other pins not under test = 0V)	$I_{I(L)}$	-5	5	μA	
OUTPUT LEAKAGE CURRENT (Output disabled, 0V ≦ V_{OUT} ≦ V_{CCQ})	$I_{O(L)}$	-5	5	μA	
OUTPUT "H" LEVEL VOLTAGE (I_{OUT} = -2 mA)	V_{OH}	2.4	-	V	
OUTPUT "L" LEVEL VOLTAGE (I_{OUT} = 2 mA)	V_{OL}	-	0.4	V	

AC CHARACTERISTICS AND OPERATING CONDITIONS

(V_{CC} = 3.3V ± 0.3V, Ta = 0° to 70°C) (Notes: 5, 6, 7)

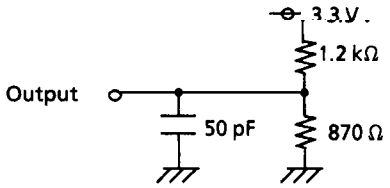
SYMBOL	PARAMETER		-8		-10		-12A		-12		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Ref/Active-Ref/Active Command Period		80		100		100		120		ns	9
t_{RAS}	Active to Precharge Command Period		48	100000	60	100000	60	100000	72	100000		
t_{RCD}	Active to Read/Write Command Delay Time		24		30		30		36			
t_{CCD}	Read/Write (a) -Read/Write (b) Command Period		8		10		12		12			
t_{RP}	Precharge to Active Command Period		24		30		30		36			
t_{RRD}	Active (a) to Active (b) Command Period		20		20		24		24			
t_{CAC}	Accesss Time from Read Command			23.5		24		24		27.5		
t_{WR}	Write Recovery Time	CL* = 1	30		30		30		36			
		CL* = 2	15		15		15		18			
		CL* = 3	1 CLK + 8		1 CLK + 10		1 CLK + 12		1 CLK + 12			
t_{CK}	CLK Cycle Time	CL* = 1	30	1000	30	1000	30	1000	36	1000		
		CL* = 2	15	1000	15	1000	15	1000	18	1000		
		CL* = 3	8	1000	10	1000	12	1000	12	1000		
t_{CH}	CLK High Level Width		3		3		4		4			10
t_{CL}	CLK Low Level Width		3		3		4		4			
t_{AC}	Access Time from CLK	CL* = 1		24		24		24		27.5		
		CL* = 2		9		9		9		9.5		
		CL* = 3		7.5		8.5		9		9		
t_{OH}	Output Data Hold Time		3		3		3		3			
t_{HZ}	Output Data High Impedance Time		3	8	3	10	3	12	3	12		8
t_{LZ}	Output Data Low Impedance Time		0		0		0		0			
t_{SB}	Power Down Mode Entry Time		0	8	0	10	0	12	0	12		
t_T	Transition Time of CLK (Rise and Fall)		1	10	1	10	1	10	1	10		
t_{DS}	Data-in Set-up Time		3		3		3		3			
t_{DH}	Data-in Hold Time		1		1		1		1			
t_{AS}	Address Set-up Time		3		3		3		3			
t_{AH}	Address Hold Time		1		1		1		1			
t_{CKS}	CKE Set-up Time		3		3		3		3			
t_{CKH}	CKE Hold Time		1		1		1		1			
t_{CMS}	Command Set-up Time		3		3		3		3			
t_{CMH}	Command Hold Time		1		1		1		1			
t_{REF}	Refresh Time			64		64		64		64	ms	
t_{RSC}	Mode Register Set Cycle Time		16		20		24		24		ns	9

* CL is $\overline{CAS}$ Latency.

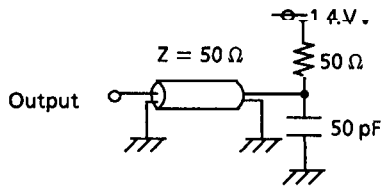
NOTES:

1. Conditions outside the limits listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device.
2. All voltages are referenced to Vss.
3. These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}. Input signals are changed once during t_{CK}.
4. These parameters depend on the output loading. Specified values are obtained with the output open.
5. Power - up sequence is described in Note 11.
6. AC TEST CONDITIONS

Output Reference Level	1.4V / 1.4V
Output Load	See diagram B below
Input Signal Levels	2.4V / 0.4V
Transition Time (Rise and Fall) of Input Signals	2ns
Input Reference Level	1.4V



AC TEST LOAD (A)



AC TEST LOAD (B)

7. Transition times are measured between V_{IH} and V_{IL}. Transition (rise and fall) of input signals have a fixed slope.
8. t_{HZ} defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.

9. These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows:

the number of clock cycles = specified value of timing / clock period
(count fractions as a whole number)

Relationship between latency and frequency (Unit: clock cycles)

-8 Version (Calculation with t_{CK} = 8ns to 24ns)

CLK period (t_{CK})	t_{RC}	t_{RAS}	t_{RP}	t_{CAC}	t_{RCD}	t_{RSC}	t_{RRD}
	80ns	48ns	24ns	23.5ns	24ns	16ns	20ns
≧ 24ns	4	2	1	2	1	1	1
≧ 16ns	5	3	2	2	2	1	2
≧ 14ns	6	4	2	3	2	2	2
≧ 12ns	7	4	2	3	2	2	2
≧ 10ns	8	5	3	3	3	2	2
≧ 9ns	9	6	3	3	3	2	3
≧ 8ns	10	6	3	3	3	2	3

-10 Version (Calculation with t_{CK} = 10ns to 30ns)

CLK period (t_{CK})	t_{RC}	t_{RAS}	t_{RP}	t_{CAC}	t_{RCD}	t_{RSC}	t_{RRD}
	100ns	60ns	30ns	24ns	30ns	20ns	20ns
≧ 30ns	4	2	1	1	1	1	1
≧ 20ns	5	3	2	2	2	1	1
≧ 18ns	6	4	2	2	2	2	2
≧ 15ns	7	4	2	2	2	2	2
≧ 13ns	8	5	3	3	3	2	2
≧ 12ns	9	5	3	3	3	2	2
≧ 10ns	10	6	3	3	3	2	2

-12A Version (Calculation with t_{CK} = 12ns to 36ns)

CLK Period (t_{CK})	t_{RC}	t_{RAS}	t_{RP}	t_{CAC}	t_{RCD}	t_{RSC}	t_{RRD}
	100ns	60ns	30ns	24ns	30ns	24ns	24ns
≧ 36ns	3	2	1	1	1	1	1
≧ 24ns	5	3	2	2	2	1	1
≧ 20ns	5	3	2	2	2	2	2
≧ 18ns	6	4	2	2	2	2	2
≧ 15ns	7	4	2	3	2	2	2
≧ 14ns	8	5	3	3	3	2	2
≧ 12ns	9	5	3	3	3	2	2

-12 Version (Calculation with t_{CK} = 12ns to 36ns)

CLK period (t_{CK})	t_{RC}	t_{RAS}	t_{RP}	t_{CAC}	t_{RCD}	t_{RSC}	t_{RRD}
	120ns	72ns	36ns	27.5ns	36ns	24ns	24ns
≧ 36ns	4	2	1	1	1	1	1
≧ 24ns	5	3	2	2	2	1	1
≧ 20ns	6	4	2	2	2	2	2
≧ 18ns	7	4	2	2	2	2	2
≧ 15ns	8	5	3	3	3	2	2
≧ 14ns	9	6	3	3	3	2	2
≧ 12ns	10	6	3	3	3	2	2

10. t_{CH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min). t_{CL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL} (max).

11. Power-up Sequence

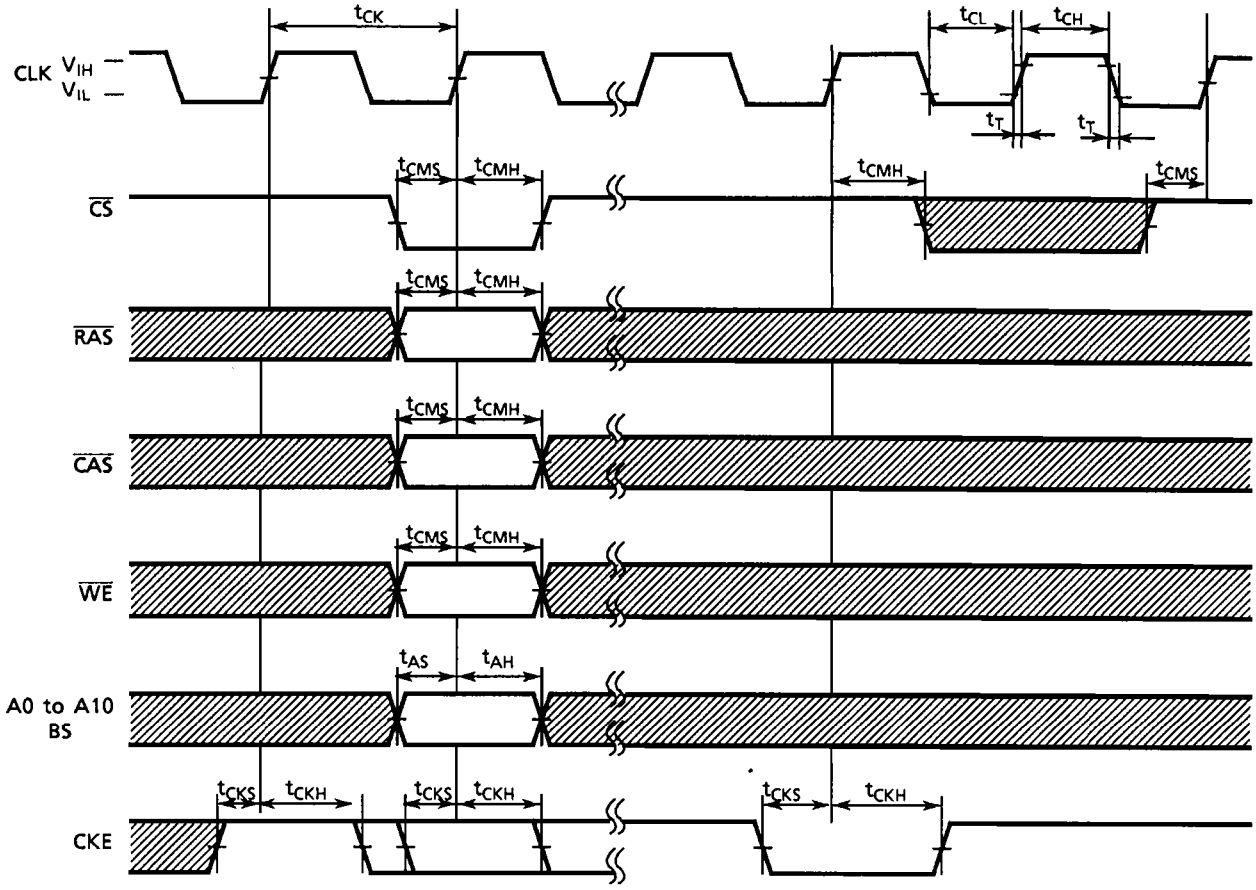
Power-up must be performed in the following sequence.

1) Power must be applied to V_{CC} and $V_{CC}Q$ (simultaneously) while all input signals are held in the "NOP" state. The CLK signal must be started at the same time.
2) After power-up a pause of at least 200 μseconds is required. It is required that DQM and CKE signals then be held "high" (V_{CC} levels) to ensure that the DQ output is high impedance.
3) Both banks must be precharged.
4) The Mode Register Set command must be asserted to initialize the Mode register.
5) A minimum of eight Auto Refresh dummy cycles is required to stabilize the internal circuitry of the device.

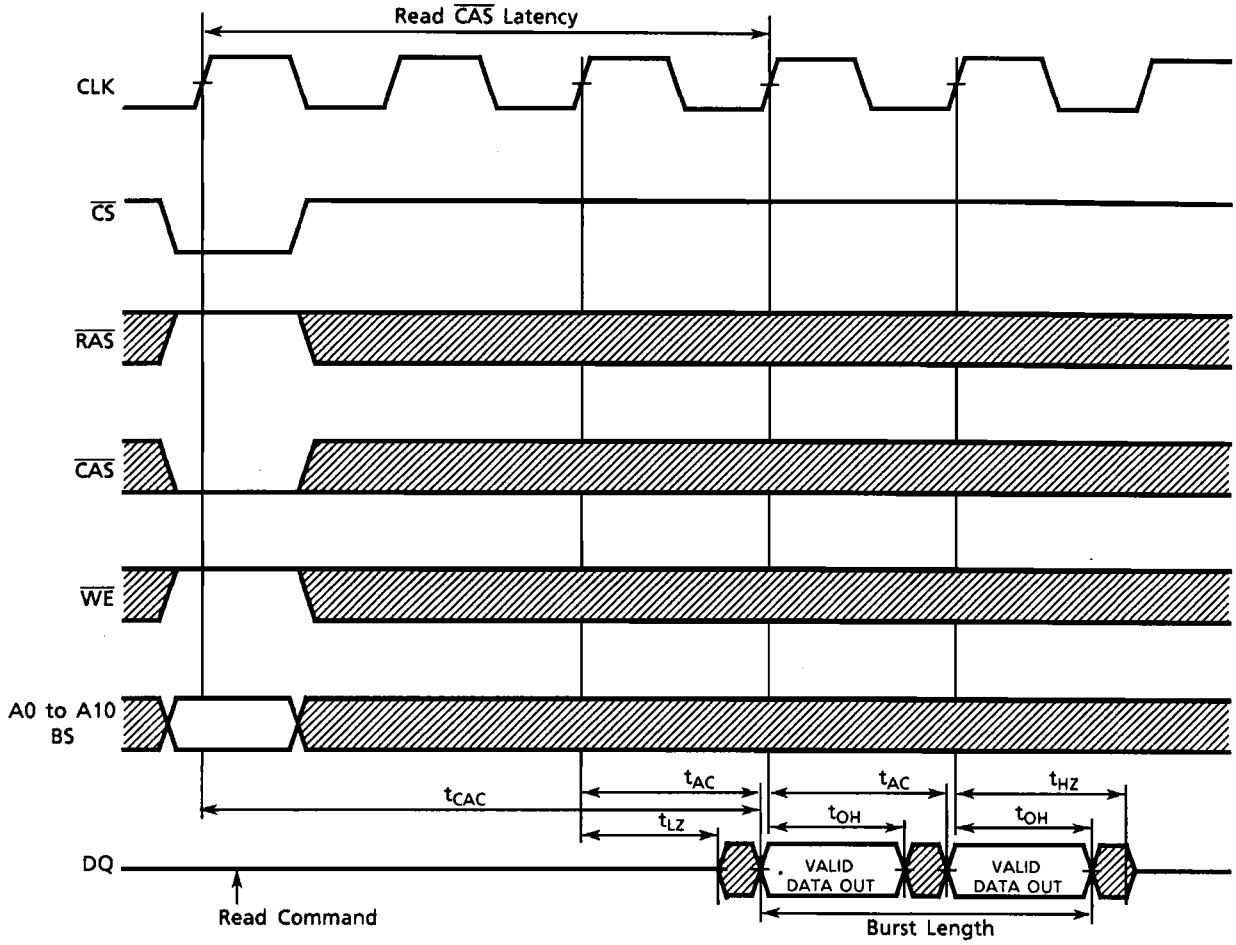
The Mode Register Set command can be invoked either before or after the Auto Refresh dummy cycles.

TIMING DIAGRAMS

Command Input Timing

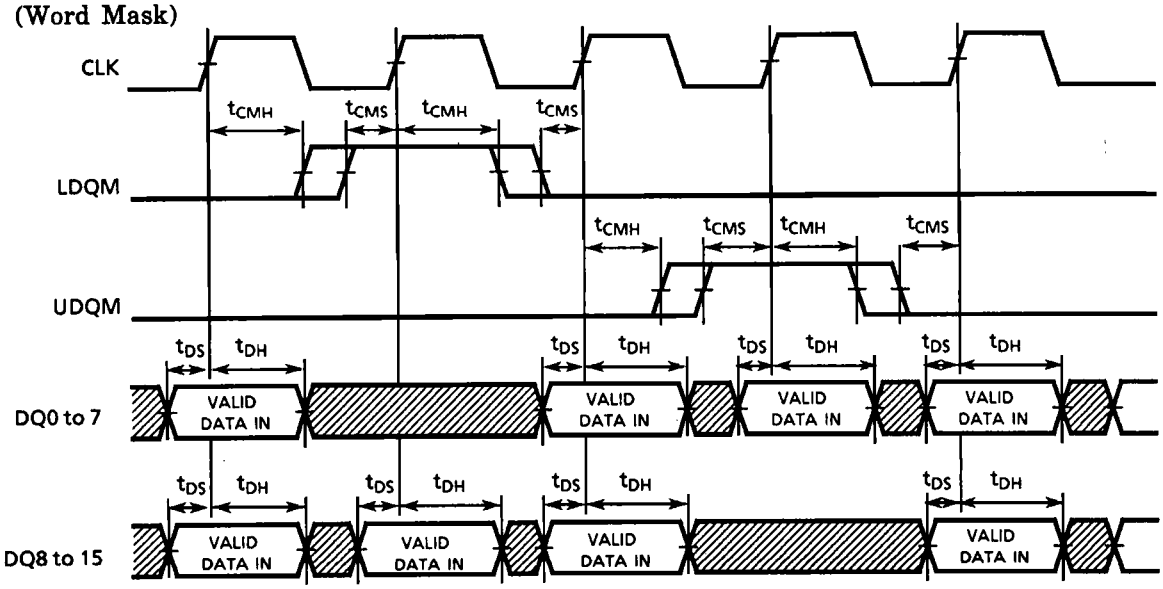


Read Timing

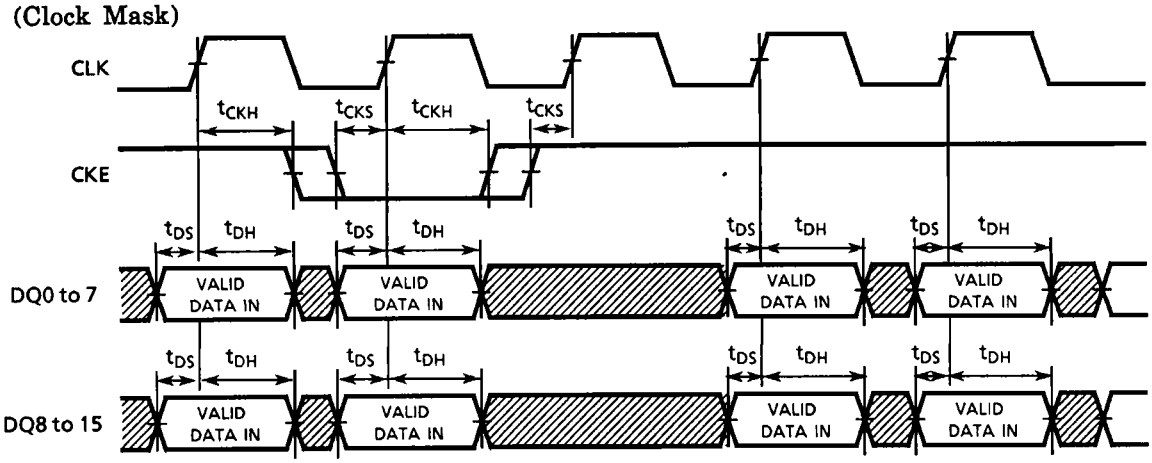

Read $\overline{CAS}$ Latency
CLK
$\overline{CS}$
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
A0 to A10
BS
t_{CAC}
t_{AC}
t_{LZ}
t_{AC}
t_{OH}
t_{HZ}
t_{OH}
DQ
VALID DATA OUT
VALID DATA OUT
Read Command
Burst Length

Control Timing of Input Data (TC59S1616AFT)

(Word Mask)

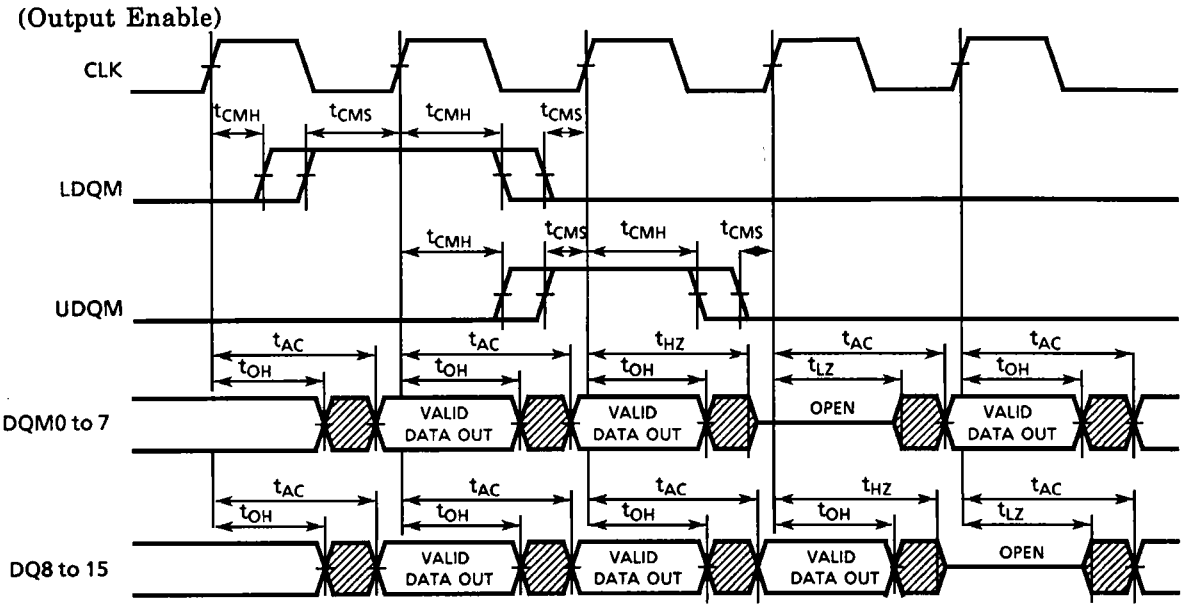


(Clock Mask)

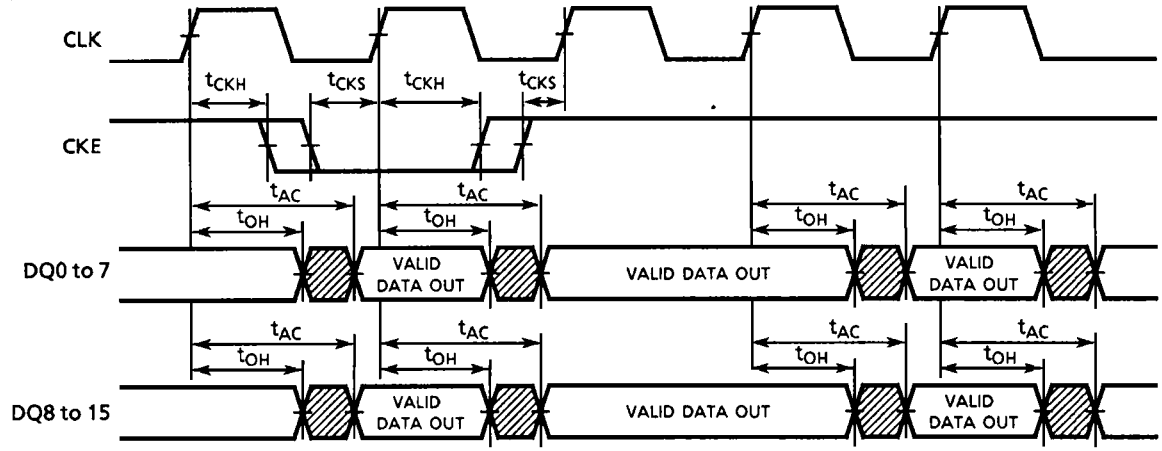


Control Timing of Output Data (TC59S1616AFT)

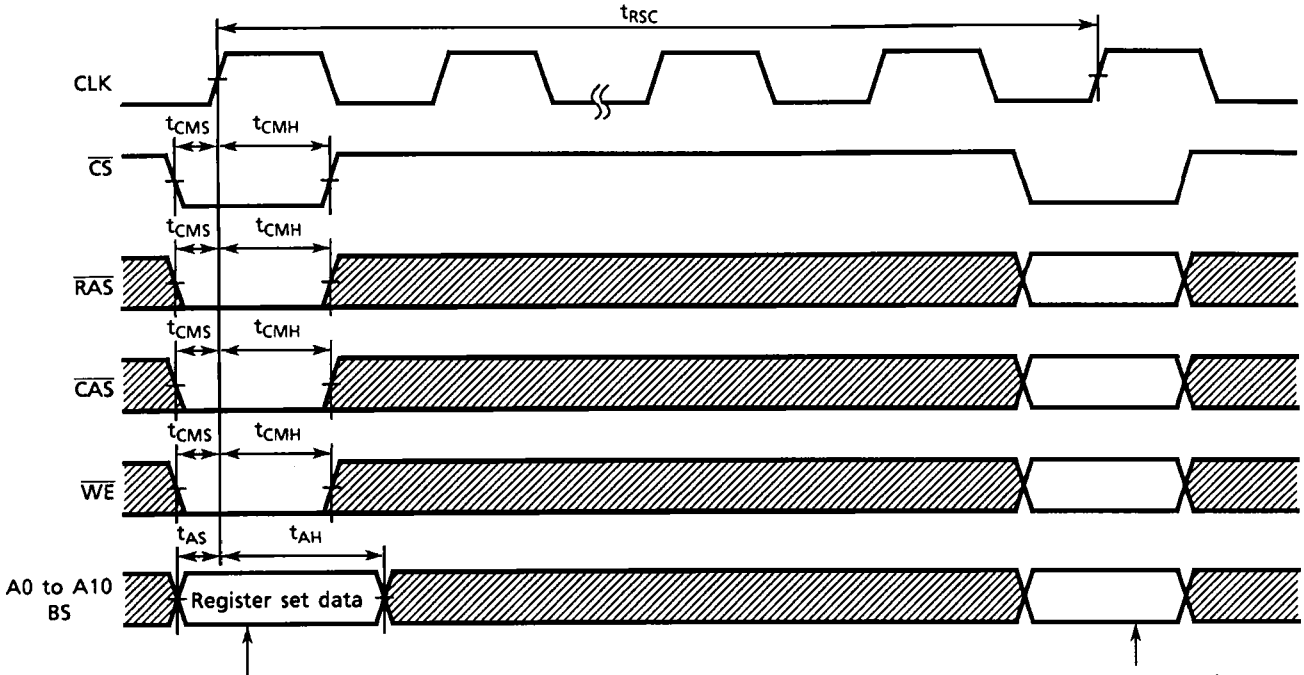
(Output Enable)



(Clock Mask)



Mode Register Set Cycle



A0	A1	A2	Burst Length
A3			Addressing Mode
A4	A5	A6	CAS Latency
A7	"0"		(Test Mode)
A8	"0"		Reserved
A9			Write Mode
A10	"0"		Reserved
BS	"0"		

	Burst Length	
A2 A1 A0	Sequential	Interleave
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1		
1 1 0		
1 1 1	Full Page	

A3	Addressing Mode
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	×	×	Reserved

A9	Single Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

OPERATING TIMING EXAMPLES (-10 Version)

Figure 1. Interleaved Bank Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)

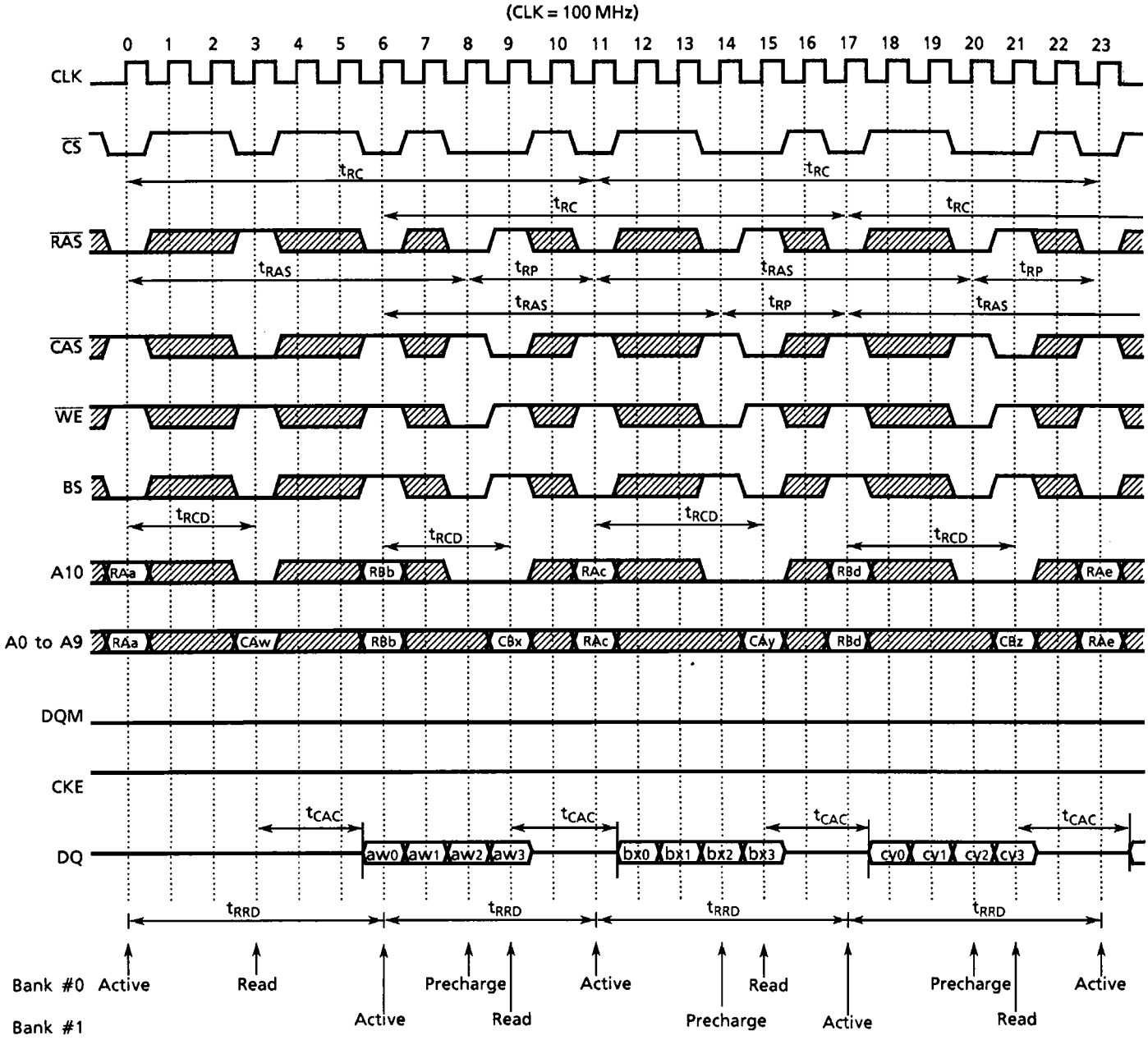
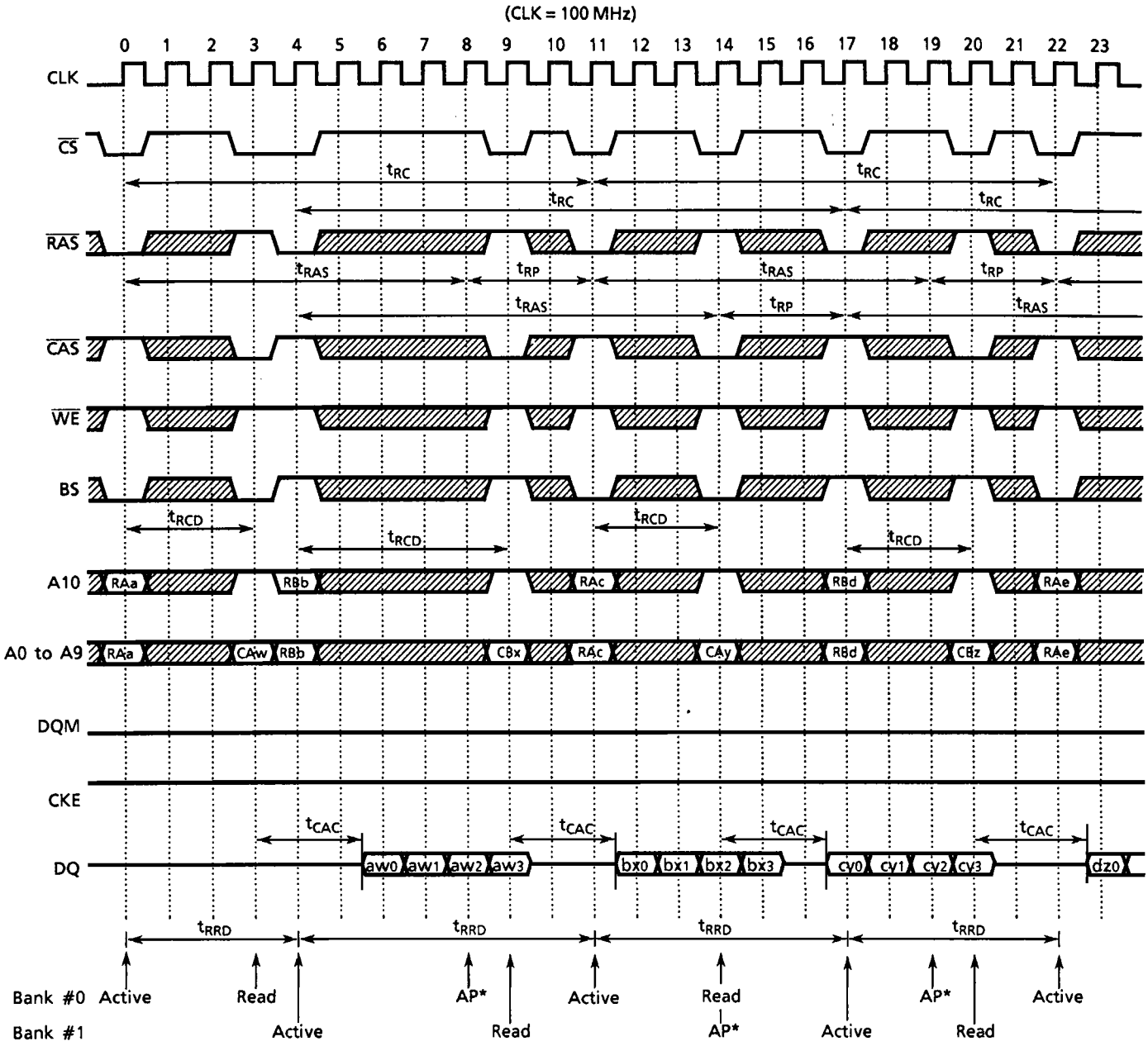


Figure 2. Interleaved Bank Read (Burst Length = 4, $\overline{CAS}$ Latency = 3, Auto Precharge)



* AP is the internal precharge start timing.

Figure 3. Interleaved Bank Read (Burst Length=8, $\overline{CAS}$ Latency=3)

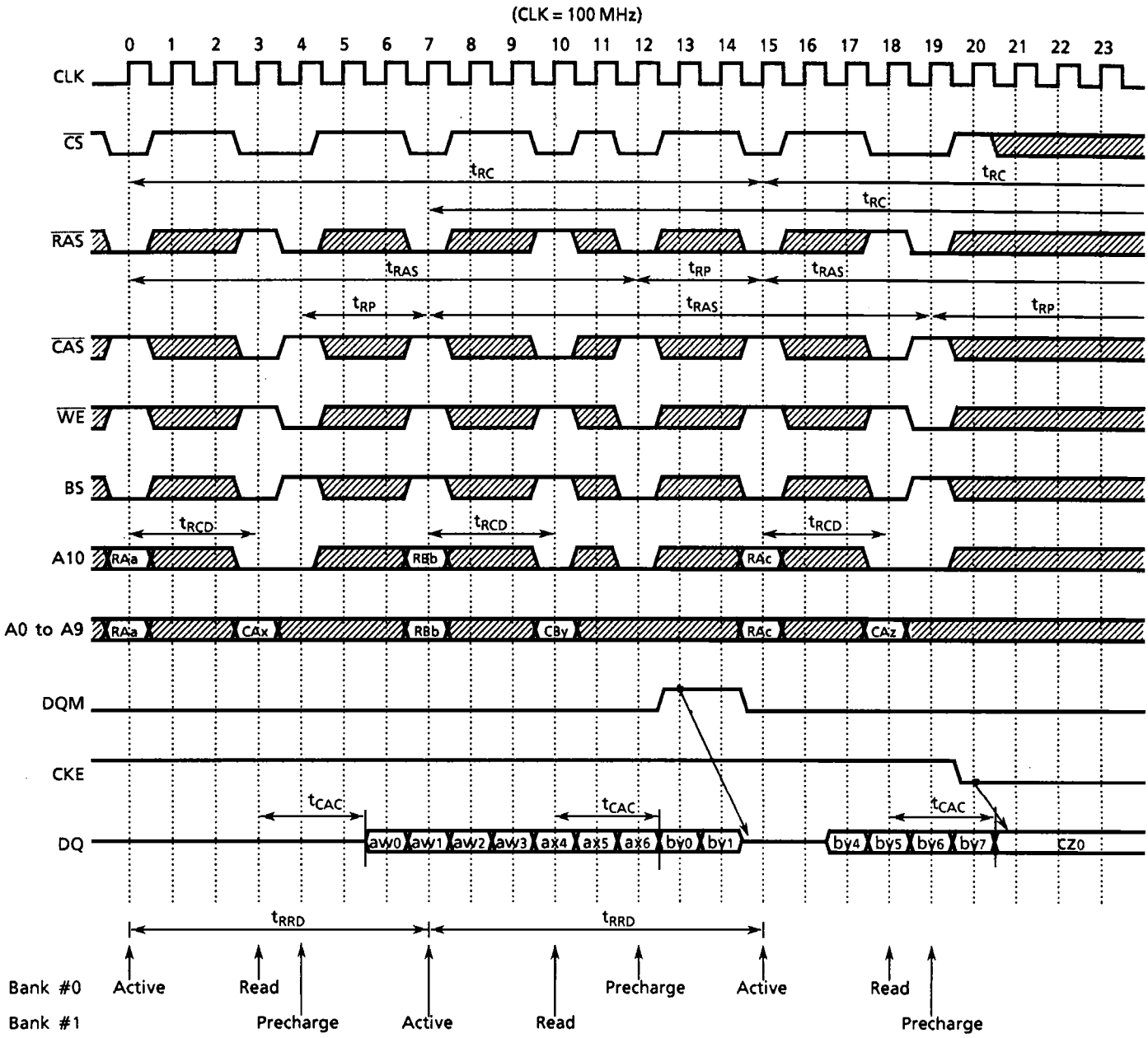
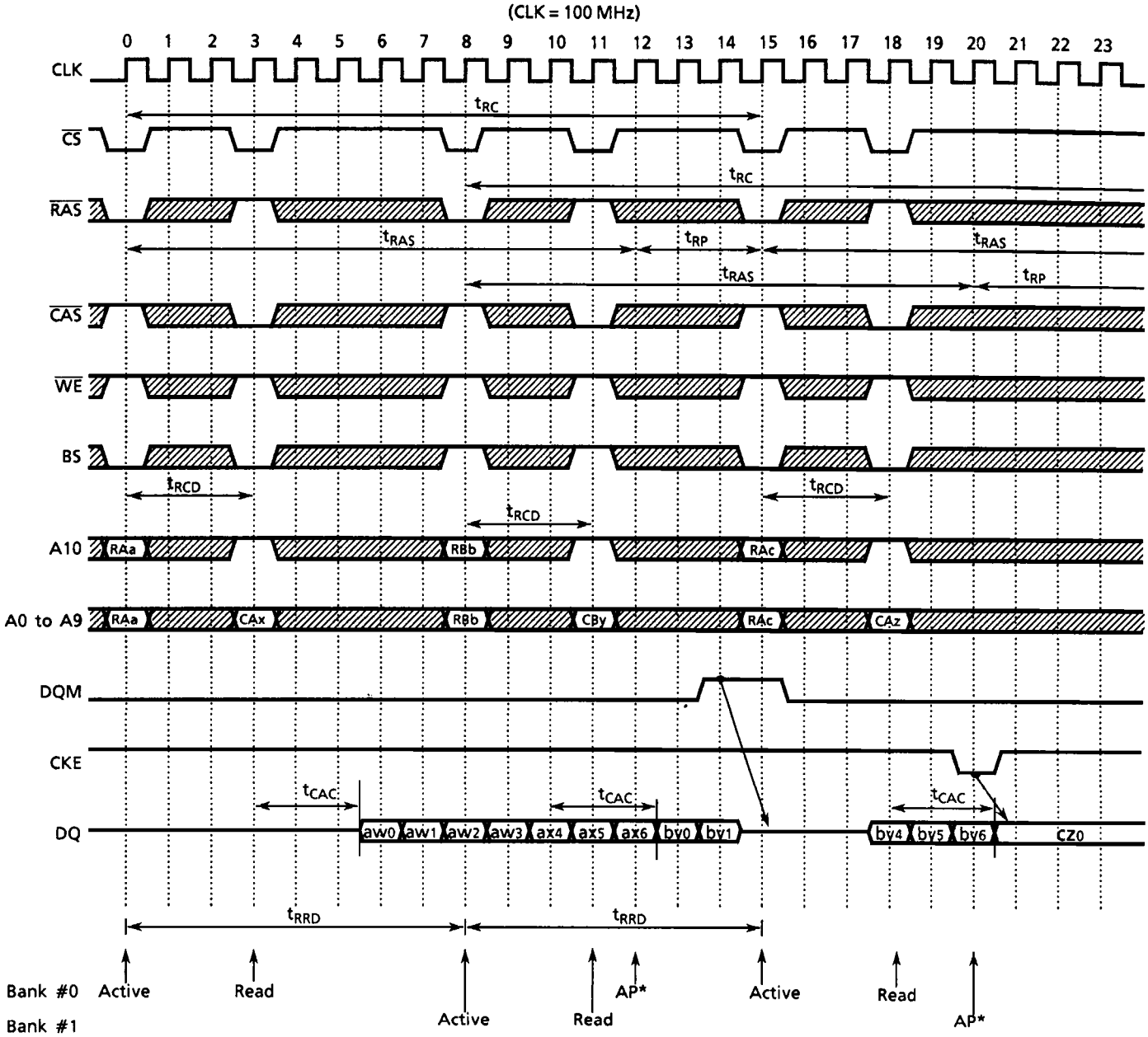


Figure 4. Interleaved Bank Read (Burst Length = 8, $\overline{CAS}$ Latency = 3, Auto Precharge)



* AP is the internal precharge start timing.

Figure 5. Interleaved Bank Write (Burst Length = 8)

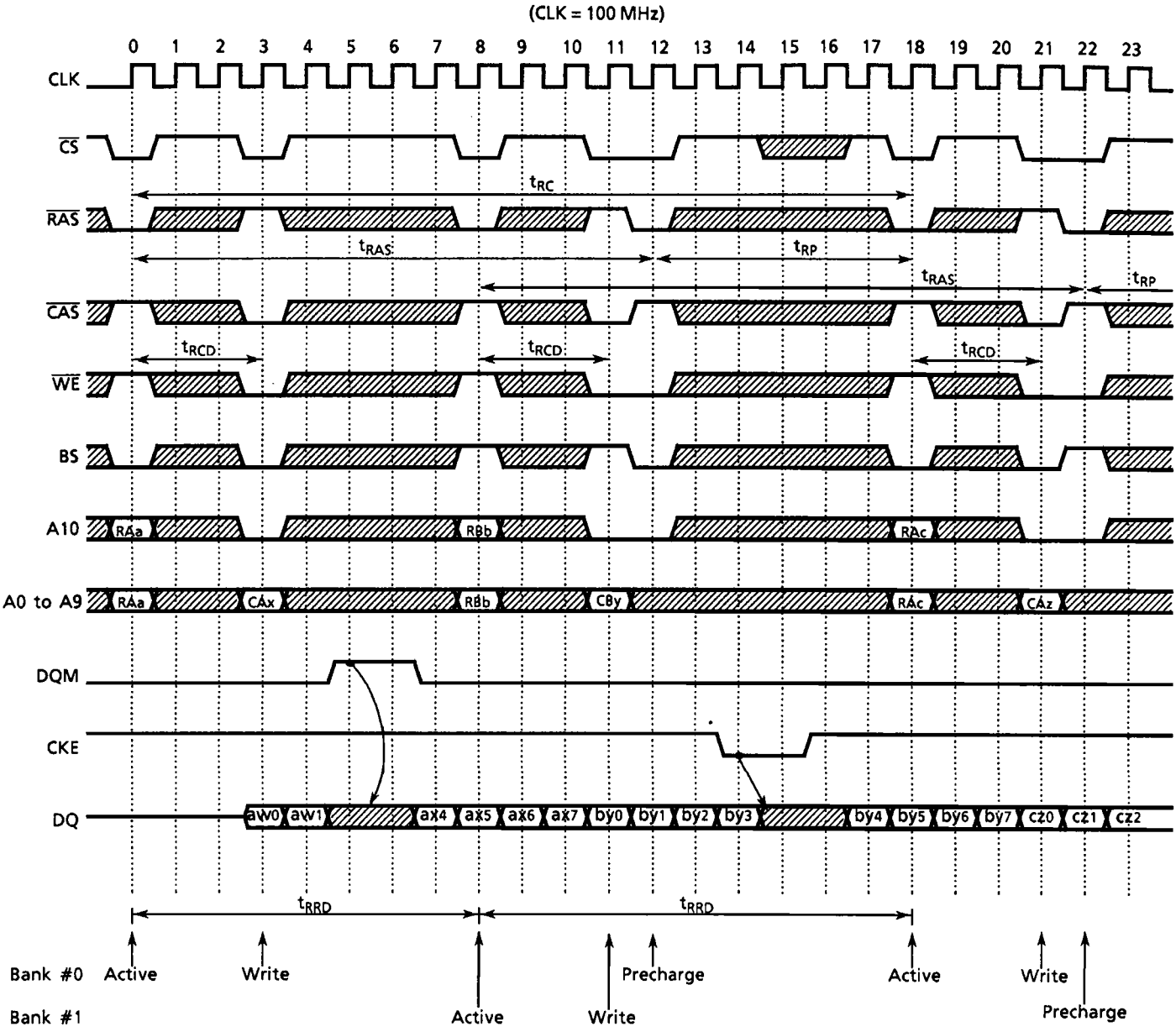
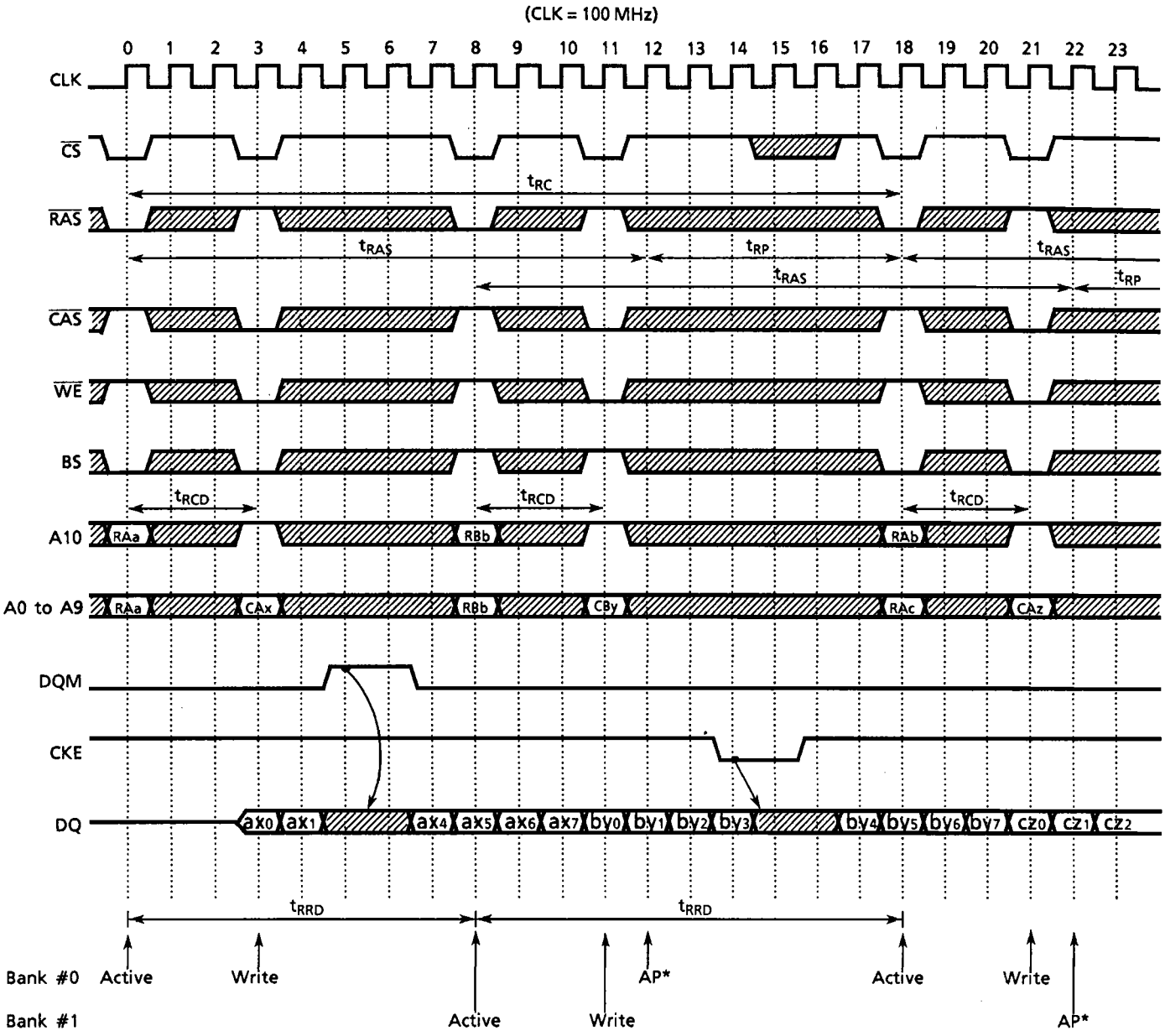
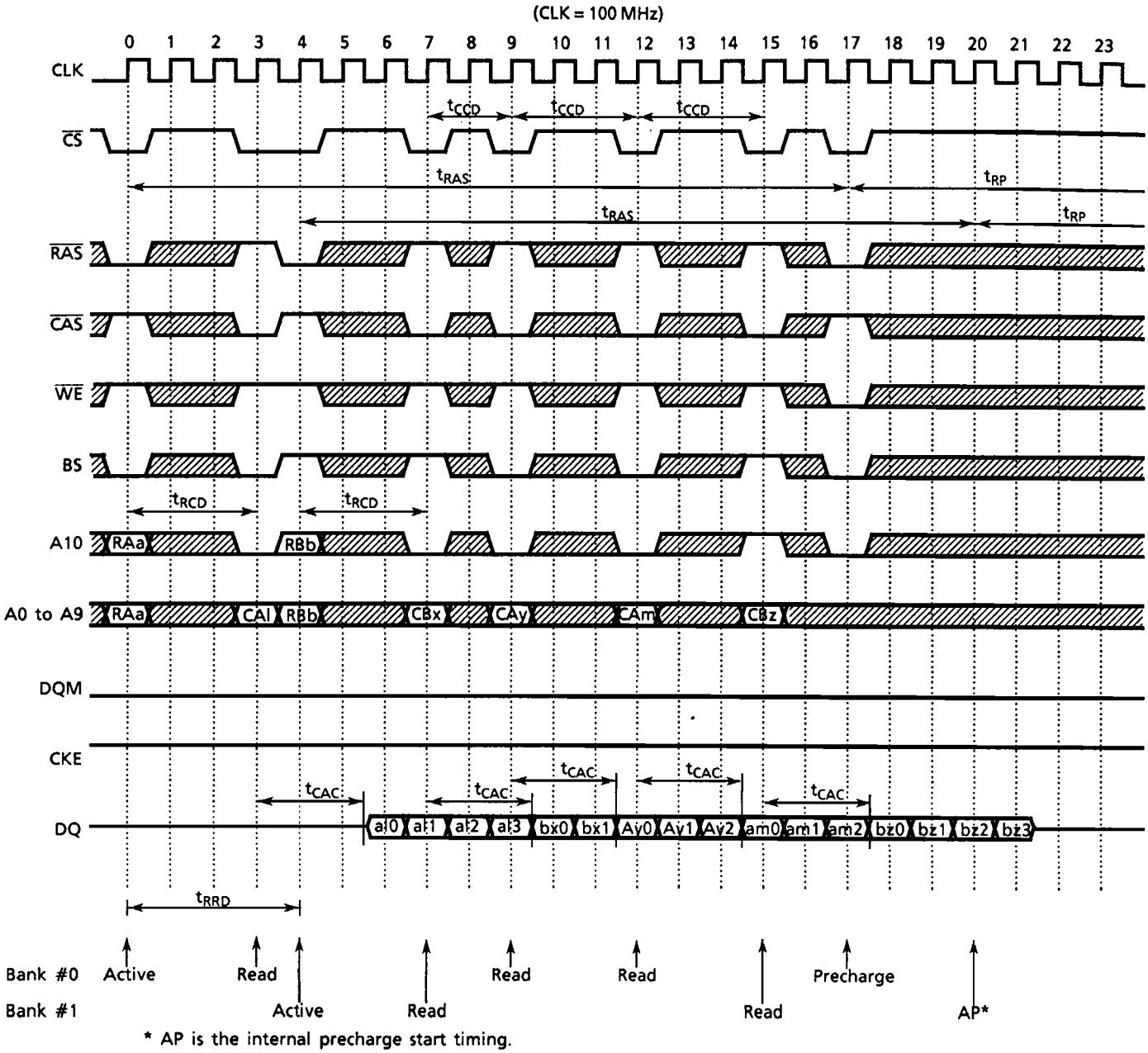


Figure 6. Interleaved Bank Write (Burst Length = 8, Auto Precharge)



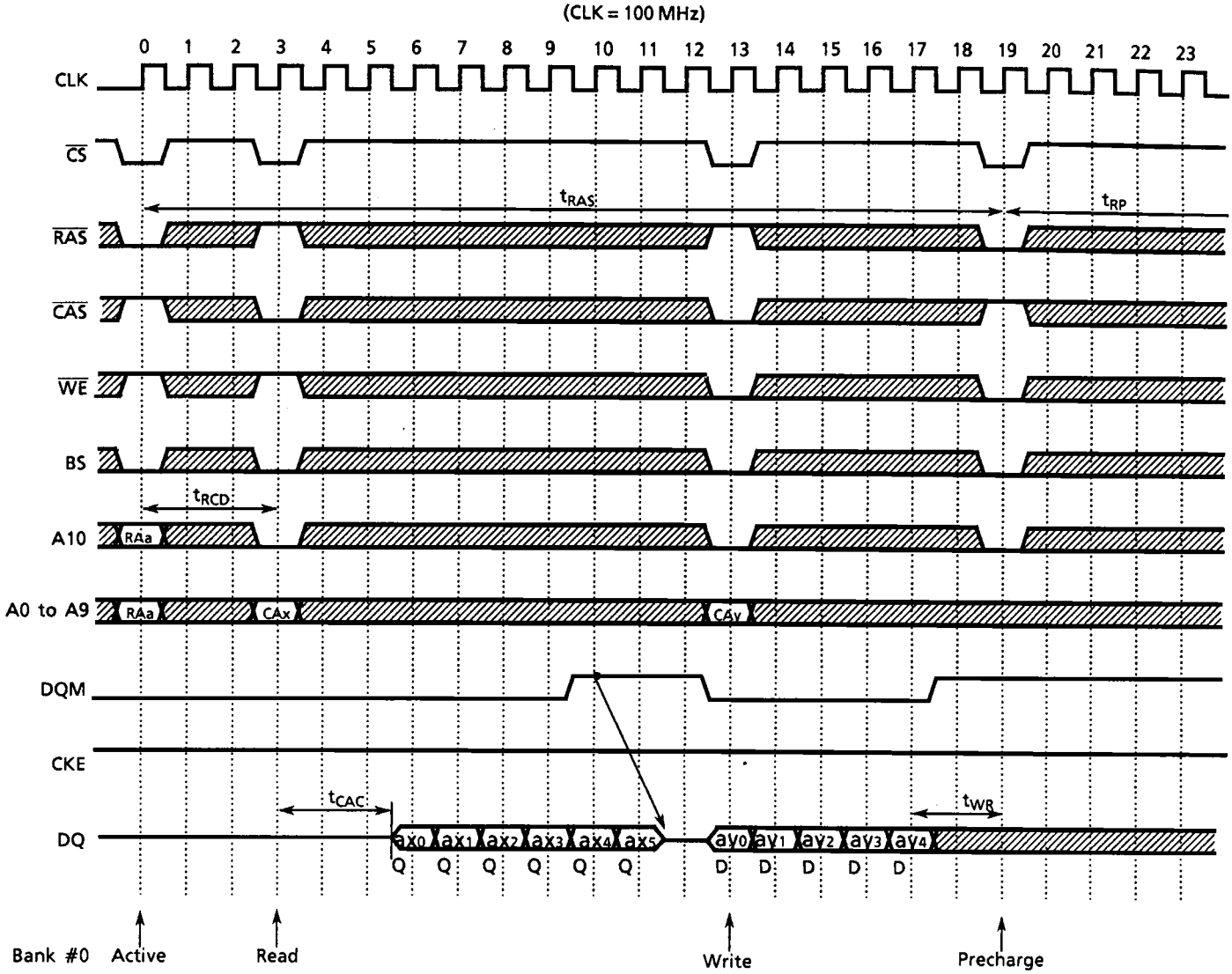
* AP is the internal precharge start timing.

Figure 7. Page Mode Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)



* AP is the internal precharge start timing.

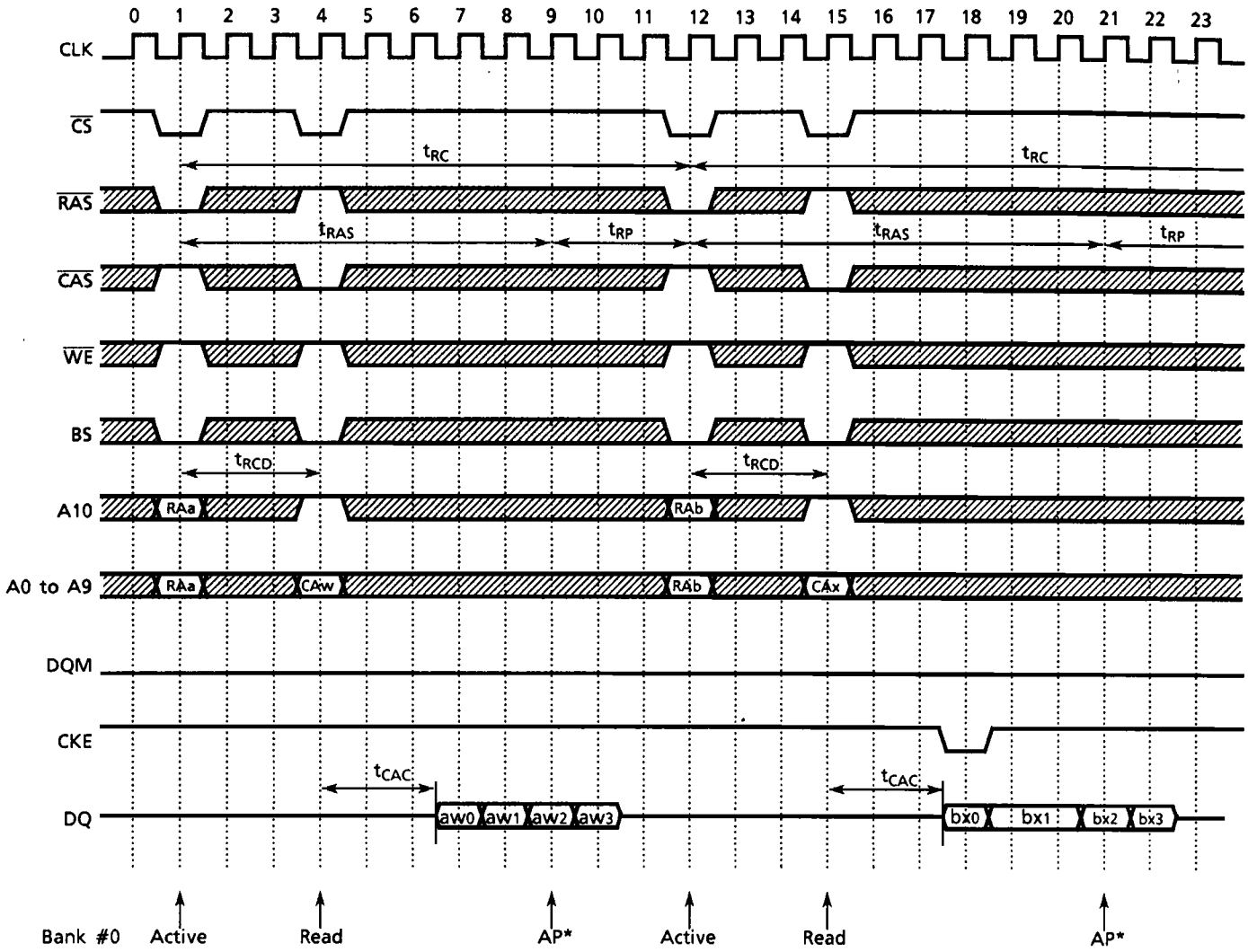
Figure 8. Page Mode Read / Write (Burst Length = 8, $\overline{CAS}$ Latency = 3)



NOTE): See Figure 17, 20

Figure 9. Auto Precharge Read (Burst Length = 4, $\overline{CAS}$ Latency = 3)

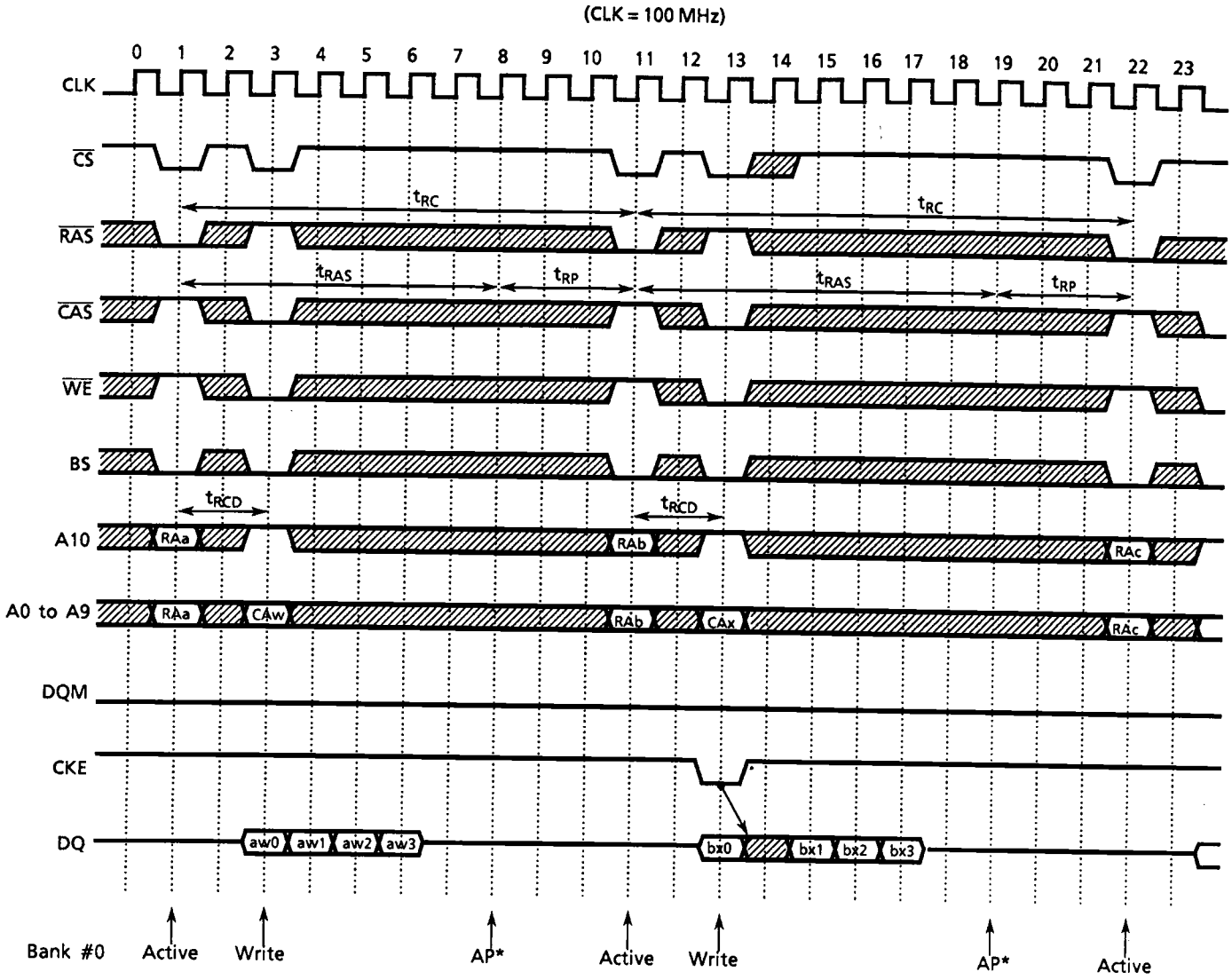
(CLK = 100 MHz)



*AP is the internal precharge start timing.

NOTE): See Figure 15

Figure 10. Auto Precharge Write (Burst Length = 4)



* AP is the internal precharge start timing.

NOTE): See Figure 16

Figure 11. Auto Refresh cycle

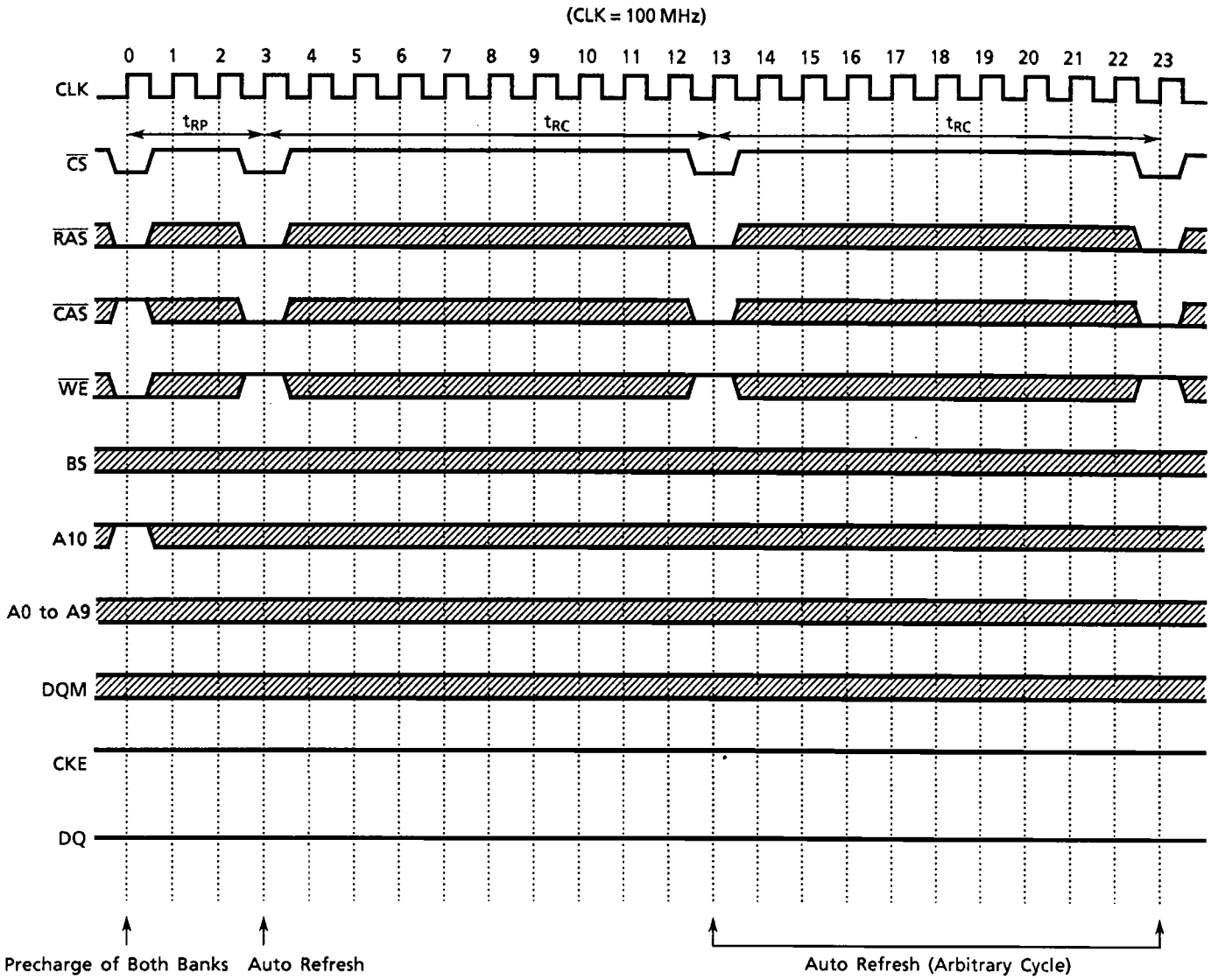


Figure 12. Self Refresh Cycle

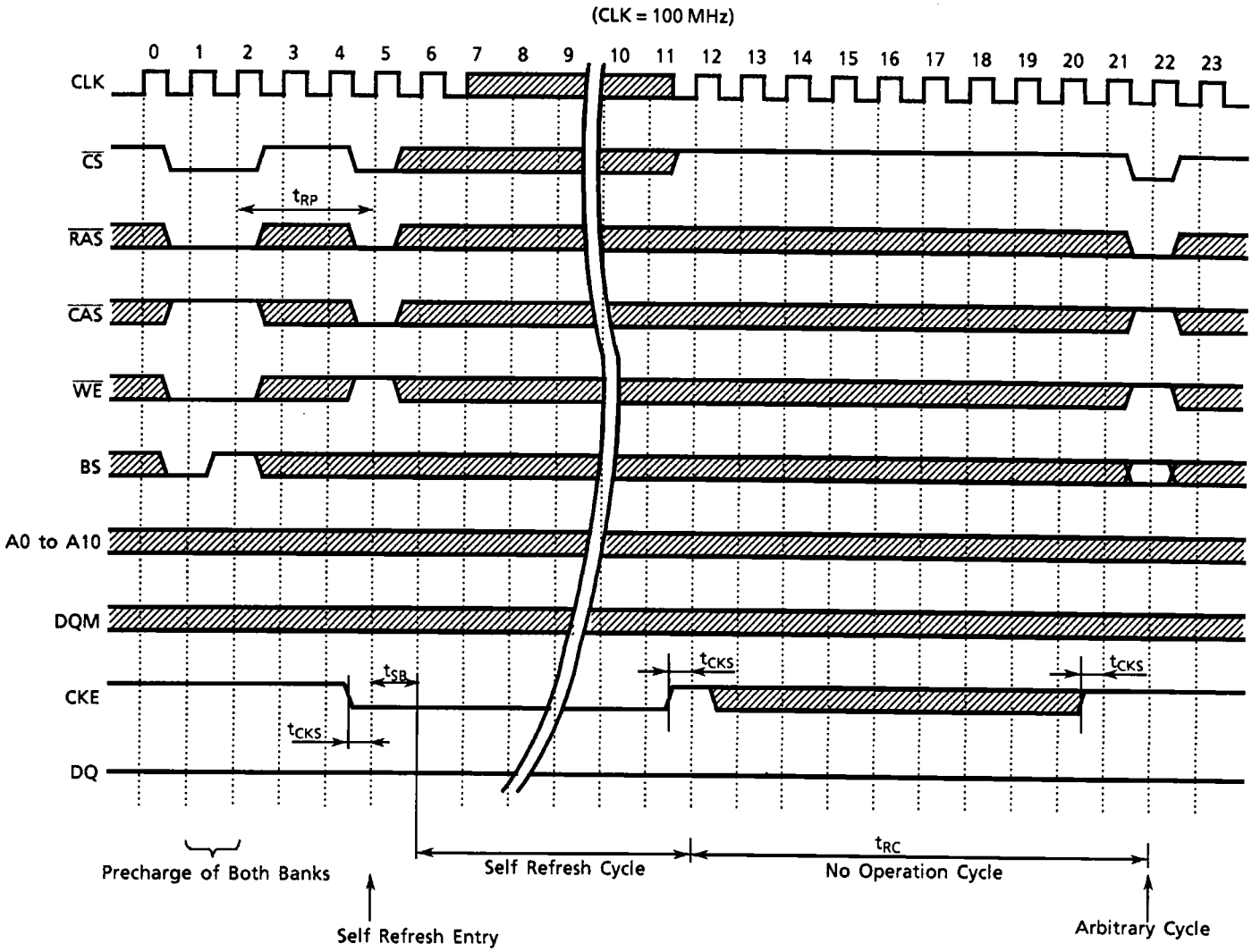
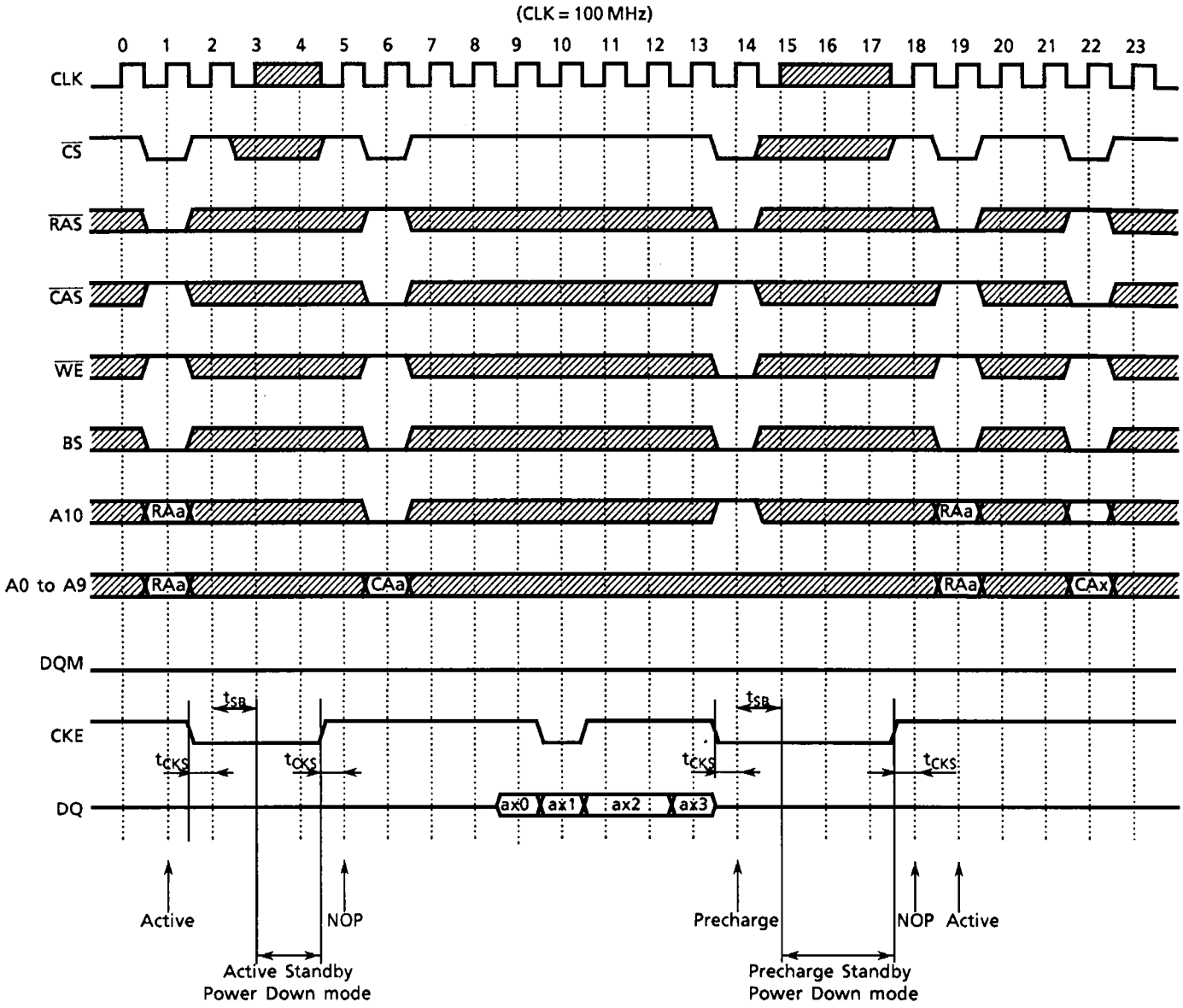
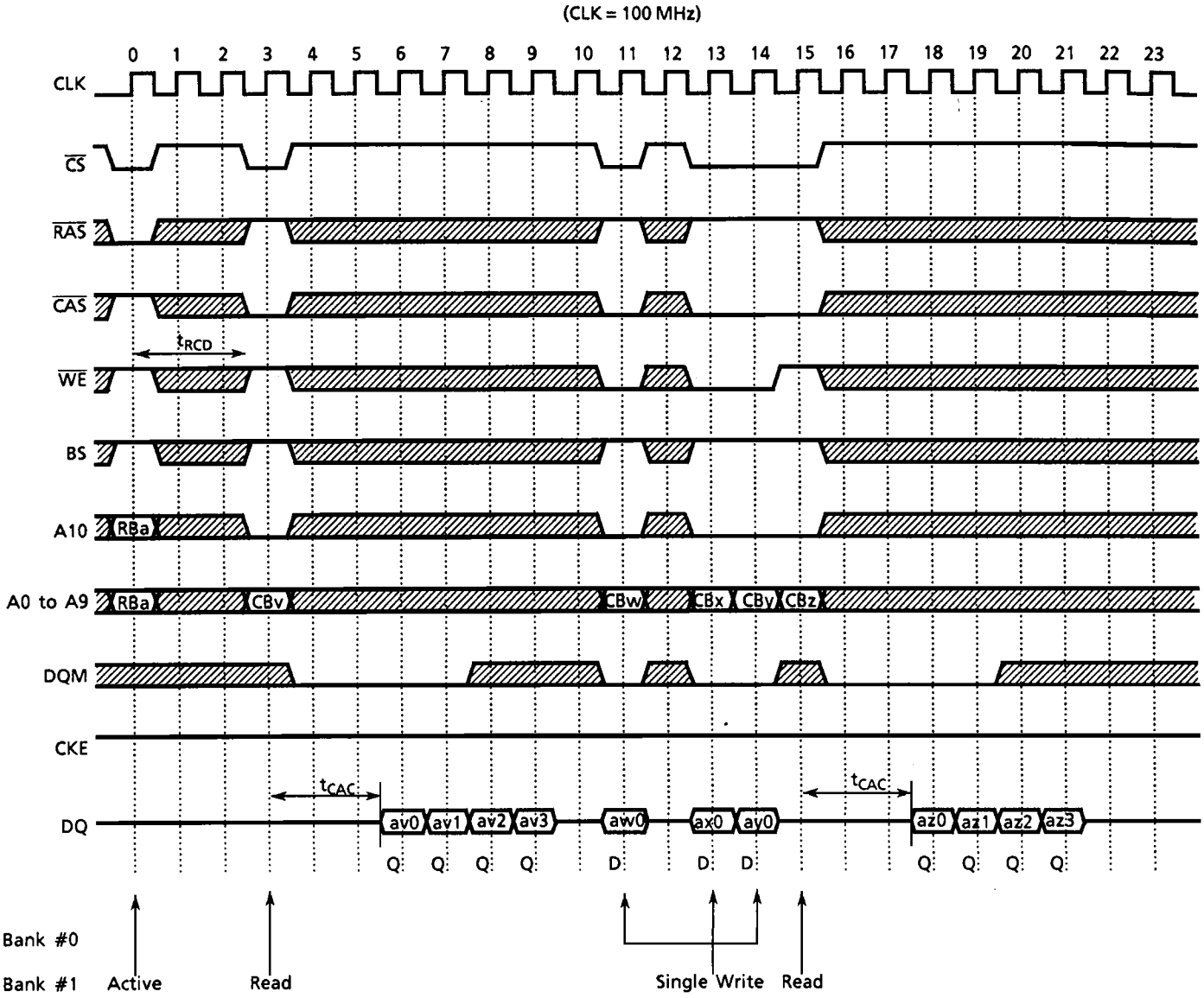


Figure 13. Power Down Mode



NOTE : The Power Down mode is invoked by asserting CKE "low".
All Input / Output buffers (except the CKE buffer) are turned off in Power Down mode.
When CKE goes high, the No-Operation command must be input on the next rising edge of CLK.

Figure 14. Burst Read and Single Write (Burst Length = 4, $\overline{CAS}$ Latency = 3)



PIN FUNCTIONS

CLOCK INPUT: CLK

The CLK input is used as the reference for S-DRAM operations. All operations are synchronized to the positive edge of CLK.

CLOCK ENABLE: CKE

The CKE input is used to suspend the internal CLK. When the CKE signal is asserted "low", the internal CLK is suspended and output data is held intact while CKE is asserted "low". When the device is not operating a Burst Cycle, the CKE input controls entry into Power Down mode.

BANK SELECT: BS

The TC59S1616AFT is organized as two-bank memory cell arrays. The BS input is latched at the time of assertion of the operation commands and selects the bank to be used for the operation. When BS is asserted "low", bank 0 is selected. When BS is asserted "high", bank 1 is selected.

ADDRESS INPUTS: A0 to A10

The A0 to A10 inputs are used to access the memory cell array, as shown in the following table.

	Row Address	Column Address
TC59S1616AFT	A0 to A10	A0 to A7

The row address bits are latched on the Bank Activate command and the column address bits are latched on the Read or Write command. Also, the A0 to A10 inputs are used to set the Mode register in a Mode Register Set cycle.

CHIP SELECT: $\overline{CS}$

The $\overline{CS}$ input controls the latching of commands on the positive edges of CLK when $\overline{CS}$ is asserted "low". No commands are latched as long as $\overline{CS}$ is held "high".

ROW ADDRESS STROBE: $\overline{RAS}$

The $\overline{RAS}$ input defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ inputs, and is latched on the positive edges of CLK. When $\overline{RAS}$ and $\overline{CS}$ are asserted "low" and $\overline{CAS}$ is asserted "high", either the Bank Activate command or the Precharge command is selected by the $\overline{WE}$ signal. When $\overline{WE}$ is asserted "high", the Bank Activate command is selected and the bank designated by BS is turned on so that it is in the active state. When $\overline{WE}$ is asserted "low", the Precharge command is selected and the bank designated by BS is switched to the idle state after the Precharge operation.

COLUMN ADDRESS STROBE: $\overline{CAS}$

The $\overline{CAS}$ input defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ inputs, and is latched on the positive edges of CLK. When $\overline{RAS}$ is held "high" and $\overline{CS}$ is asserted "low", column access is started by asserting $\overline{CAS}$ "low". Then, the Read or Write command is selected by asserting $\overline{WE}$ "low" or "high".

WRITE ENABLE: $\overline{WE}$

The $\overline{WE}$ input defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ inputs, and is latched on the positive edges of CLK. The $\overline{WE}$ input is used to select the Bank Activate or Precharge command, and Read or Write command.

DATA INPUT/OUTPUT MASK: DQM or L-DQM and U-DQM

The DQM input enables output in a Read cycle and functions as the input data mask in a Write cycle. When DQM is asserted "high" on the positive edges of CLK, output data is disabled after two clock cycles during a Read cycle, and input data is masked on the same clock cycle during a Write cycle.

In the case of the TC59S1616AFT, the LDQM and UDQM inputs function as byte data control. The LDQM input can control DQ0-7 in a Read or Write cycle and the UDQM can control DQ8-15 in a Read or Write cycle.

DATA INPUT/OUTPUT: DQ0-15

The DQ0-15 input and output data are synchronized with the positive edges of CLK.

Operation Mode

Fully synchronous operations are performed to latch the commands on the positive edges of CLK. Table 1 shows the truth table for the operation commands.

Table 1 Truth Table (Notes (1) and (2))

Command	Device State	CKE_{n-1}	CKE_n	DQM(5)	BS	A10	A9-0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Bank Activate	Idle (3)	H	×	×	V	V	V	L	L	H	H
Bank Precharge	Any	H	×	×	V	L	×	L	L	H	L
Precharge All	Any	H	×	×	×	H	×	L	L	H	L
Write	Active (3)	H	×	×	V	L	V	L	H	L	L
Write with Auto Precharge	Active (3)	H	×	×	V	H	V	L	H	L	L
Read	Active (3)	H	×	×	V	L	V	L	H	L	H
Read with Auto Precharge	Active (3)	H	×	×	V	H	V	L	H	L	H
Mode Register Set	Idle	H	×	×	V	V	V	L	L	L	L
No-Operation	Any	H	×	×	×	×	×	L	H	H	H
Burst stop	Active (4)	H	×	×	×	×	×	L	H	H	L
Device Deselect	Any	H	×	×	×	×	×	H	×	×	×
Auto Refresh	Idle	H	H	×	×	×	×	L	L	L	H
Self Refresh Entry	Idle	H	L	×	×	×	×	L	L	L	H
Self Refresh Exit	Idle (Self Refresh)	L	H	×	×	×	×	H	×	×	×
								L	H	H	×
Clock Suspend Mode Entry	Active	H	L	×	×	×	×	×	×	×	×
Power Down Mode Entry	Any (6)	H	L	×	×	×	×	H	×	×	×
								L	H	H	×
Clock Suspend Mode Exit	Active	L	H	×	×	×	×	×	×	×	×
Power Down Mode Exit	Any (Power Down)	L	H	×	×	×	×	H	×	×	×
								L	H	H	×
Data Write/Output Enable	Active	H	×	L	×	×	×	×	×	×	×
Data Write/Output Disable	Active	H	×	H	×	×	×	×	×	×	×

Note (1) V = Valid × = Don't Care L = Low level H = High level

(2) CKE_n signal is input level when commands are issued.
CKE_{n-1} signal is input level one clock cycle before the commands are issued.

(3) The bank state designated by the BS signal.

(4) Device state is Full Page Burst operation.

(5) LDQM, UDQM (TC59S1616AFT)

(6) Device state is not Burst operation.

1. Command functions

1 - 1 Bank Activate command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "H", BS = Bank, A0 to A10 = Row Address)

The Bank Activate command activates the bank designated by the BS (Bank Select) signal. Row addresses are latched on A0 to A10 when this command is issued and the cell data is read out of the sense amplifiers. The maximum time that each bank can be held in the active state is as specified by $t_{RAS\,(max)}$.

1 - 2 Bank Precharge command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "L", BS = Bank, A10 = "L", A0 to A9 = "Don't care")

The Bank Precharge command precharges the bank designated by BS. The precharged bank is switched from the active state to the idle state.

1 - 3 Precharge All command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "L", BS = "Don't care", A10 = "H", A0 to A9 = "Don't care")

The Precharge All command precharges both banks simultaneously. Both banks are then switched to the idle state.

1 - 4 Write command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BS = Bank, A10 = "L", A0 to A9 = Column Address)

The Write command performs a Write operation to the bank designated by BS. The write data is latched on the positive edges of CLK. The lengths of the write data (Burst Length) and column access sequence (Addressing mode) must be set in the Mode register at power - up prior to the Write operation.

The A8 and A9 inputs are "Don't care" on the TC59S1616AFT.

1 - 5 Write with Auto Precharge command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BS = Bank, A10 = "H", A0 to A9 = Column Address)

The Write with Auto Precharge command performs the Precharge operation automatically after the Write operation. This command must not be interrupted by any other commands.

The A8 and A9 inputs are "Don't care" on the TC59S1616AFT.

1 - 6 Read command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", BS = Bank, A10 = "L", A0 to A9 = Column Address)

The Read command performs a Read operation on the bank designated by BS. The read data is issued sequentially synchronized to the positive edges of CLK. The length of the read data (Burst Length), Addressing mode and $\overline{CAS}$ latency (access time from $\overline{CAS}$ command in a clock cycle) must be programmed in the Mode register at power-up prior to the Write operation.

The A8 and A9 inputs are "Don't care" on the TC59S1616AFT.

1 - 7 Read with Auto Precharge command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", BS=Bank, A10= "H", A0 to A9=Column Address)

The Read with Auto Precharge command automatically performs the Precharge operation after the Read operation. This command must not be interrupted by any other command.

The A8 and A9 inputs are "Don't care" on the TC59S1616AFT.

1 - 8 Mode Register Set command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BS, A0 to A10=Register Data)

The Mode Register Set command sets the values of the $\overline{CAS}$ latency, Addressing mode and Burst Length in the Mode register. The default values in the Mode register after power-up are undefined, therefore this command must be issued during the power-up sequence. Also, this command can be issued while both banks are in the idle state.

1 - 9 No-Operation command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "H", $\overline{WE}$ = "H")

The No-Operation command simply performs no operation (the same as Device Deselect).

1 - 10 Burst Stop command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "H", $\overline{WE}$ = "L")

The Burst Stop command is used to stop a burst operation. This command is valid during a Full Page Burst operation. During other types of Burst operation, the command is illegal.

1 - 11 Device Deselect command

($\overline{CS}$ = "H")

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

1 - 12 Auto Refresh command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", CKE= "H", BS, A0 to A10="Don't care")

The Auto Refresh command is used to refresh the row address provided by the internal refresh counter. Both banks (#0 and #1) are refreshed alternately by the Auto Refresh command and the refresh counter is automatically incremented. The Refresh operation must be performed 4096 times within 64ms. The next command can then be issued t_{RC} after the end of the Auto Refresh command. When the Auto Refresh command is issued, both banks must be in the idle state. The Auto Refresh operation is equivalent to the $\overline{CAS}$-before-$\overline{RAS}$ operation in a conventional DRAM.

1 - 13 Self Refresh Entry command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", CKE = "L", BS, A0 to A10 = "Don't care")

The Self Refresh Entry command is used to enter Self Refresh mode. While the device is in Self Refresh mode, all input and output buffers (except the CKE buffer) are disabled and the Refresh operation is automatically performed. Self Refresh mode is exited by taking CKE "high" (the Self Refresh Exit command)

1 - 14 Self Refresh Exit command

(CKE = "H", $\overline{CS}$ = "H" or CKE = "H", $\overline{RAS}$ = "H", $\overline{CAS}$ = "H")

This command is used to exit from Self Refresh mode. Any subsequent commands can be issued t_{RC} after the end of this command.

1 - 15 Clock Suspend Mode Entry / Power Down Mode Entry command

(CKE = "L")

The internal CLK is suspended for one cycle when this command is issued (when CKE is asserted "low"). The device state remains unchanged while the CLK is suspended. Alternatively, when the device is not running a Burst cycle, this command performs entry into Power Down mode. All input and output buffers (except the CKE buffer) are turned off in Power Down mode.

1 - 16 Clock Suspend Mode Exit / Power Down Mode Exit command

(CKE = "H")

When the internal CLK has been suspended, operation of the internal CLK is resumed by invoking this command (asserting CKE "high"). When the device is in Power Down mode, the device exits this mode and all disabled buffers are put into the active state. Any subsequent commands can be issued one clock cycle after the end of this command.

1 - 17 Data Write / Output Enable, Data Mask / Output Disable command

(DQM = "L" / "H" or LDQM, UDQM = "L" / "H")

During a Write cycle, the LDQM and UDQM signals function as data mask and can control every word of the input data. During a Read cycle, the LDQM and UDQM signals control the output buffers.

The LDQM signal controls DQ0 to 7 and the UDQM signal controls DQ8 to 15.

2. Read operation

Issuing the Bank Activate command to the idle bank puts it into the active state. When the Read command is issued t_{RCD} after the Bank Activate command, the data is read out sequentially, synchronized to the positive edges of CLK (a Burst Read operation). The initial read data becomes available after a time period of t_{CAC} in clock cycles from the issuing of the Read command. The value of t_{CAC} in clock cycles ($\overline{CAS}$ latency) must be set in the Mode register at power-up. In addition, the burst length of the read data and Addressing mode must be set. Each bank is held in the active state unless the Precharge command is issued, so that the sense amplifiers can be used as a secondary cache.

When the Read with Auto Precharge command is issued, the Precharge operation is performed automatically after the Read cycle, then the bank is switched to the idle state. This command cannot be interrupted by any other commands. Also, when the Burst Length is 1 plus t_{RCD} (min), the timing from the $\overline{RAS}$ command to the start of the Auto Precharge operation is shorter than t_{RAS} (min). In this case, t_{RAS} (min) must be satisfied by extending t_{RCD} (Figure 9, 15).

When the Precharge operation is performed on a bank during a Burst Read operation, the Burst operation is terminated (Figure 20).

When the Burst Length is full-page, column data is repeatedly read out until the Burst Stop command or Precharge command is issued.

3. Write operation

Issuing the write command t_{RCD} after the Bank Activate command sequentially latches the input data, synchronizing with the positive edges of CLK after the Write command (Burst Write operation). The burst length of the Write data (Burst Length) and Addressing mode must be set in the Mode register at power-up.

When the Write with Auto Precharge command is issued, the Precharge operation is performed automatically after the Write cycle, then the bank is switched to the idle state. This command cannot be interrupted by any other command for the entire burst data duration. Also, when the Burst Length is 1 plus t_{RCD} (min), the timing from the $\overline{RAS}$ command to the start of the Auto Precharge operation is shorter than t_{RAS} (min). In this case, t_{RAS} (min) must be satisfied by extending t_{RCD} (Figure 10, 16).

When the Precharge operation is performed in a bank during a Burst Write operation, the Burst operation is terminated (Figure 20).

When the Burst Length is full-page, the input data is repeatedly latched until the Burst Stop command or the Precharge command is issued.

When Burst Read and Single Write mode is selected, the write burst length is 1 regardless of the read burst length.

4. Precharge

There are two commands which perform the Precharge operation: Bank Precharge and Precharge All. When the Bank Precharge command is issued to the active bank, the bank is precharged and then switched to the idle state. The Bank Precharge command can precharge one bank independently of the other bank and hold the unprecharged bank in the active state. The maximum time each bank can be held in the active state is specified by t_{RAS} (max). Therefore, each bank must be precharged within t_{RAS} (max) from the Bank Activate command.

The Precharge All command can be used to precharge both banks simultaneously. Even if both banks are not in the active state, the Precharge All command can still be issued. In this case, the Precharge operation is performed only on the active bank and the precharged bank is then switched to the idle state.

5. Page mode

The Read or Write command can be issued on any clock cycle.

Whenever a Read operation is to be interrupted by a Write command, the output data must be masked by DQM to avoid I/O conflict. Also, when a Write operation is to be interrupted by a Read command, only the input data before the Read command is enabled; the input data after the Read command is disabled.

6. Burst Termination

When the Precharge command is issued for a bank in a Burst cycle, the Burst operation is terminated. When the Burst Read cycle is interrupted by the Precharge command, read operation is disabled the number of clock cycles after the Precharge command equal to the $\overline{CAS}$ latency-1 (Figure 20). When the Burst Write cycle is interrupted by the Precharge command, the input circuit is reset on the same clock cycle on which the Precharge command is issued. In this case, the DQM signal must be asserted "High" to prevent writing of invalid data to the cell array (Figure 20).

When the Burst Stop command is issued for the bank in a Full-page Burst cycle, the Burst operation is terminated. When the Burst Stop command is issued during a Full-page Burst Read cycle, read operation is disabled the number of clock cycles after the Burst Stop command equal to the $\overline{CAS}$ latency-1. When the Burst Stop command is issued during a Full-page Burst Write cycle, write operation is disabled on the same clock cycle on which the Burst Stop command is issued (Figure 19).

7. Mode register operation

The Mode register designates the operation mode for the Read or Write cycle. This register is divided into three fields; A Burst Length field to set the length of the burst data, Addressing Mode select bits to designate the column access sequence in a Burst cycle, and a $\overline{\text{CAS}}$ Latency field to set the access time in clock cycles.

The Mode register is programmed by the Mode Register Set command when both banks are in the idle state. The data to be set in the Mode register is transferred using the A0 to A10 address inputs. The initial value of the Mode register after power - up is undefined; therefore the Mode Register Set command must be issued before proper operation.

- Burst Length field (A2 to A0)

This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 1, 2, 4 or 8 words, or full-page.

A2	A1	A0	Burst Length
0	0	0	1 word
0	0	1	2 words
0	1	0	4 words
0	1	1	8 words
1	1	1	Full-page

- Addressing Mode select (A3)

The Addressing mode can be one of two modes; Interleave mode or Sequential mode. When the A3 bit is "0", Sequential mode is selected. When the A3 bit is "1", Interleave mode is selected. Both Addressing modes support burst lengths of 1, 2, 4 and 8 words. Additionally, Sequential mode supports full-page bursts.

A3	Addressing Mode
0	Sequential
1	Interleave

Table 2 Addressing sequence for Sequential mode

Data	Access Address	Burst Length
Data 0	n	2 words (Address bit is A0) no carry from A0 to A1 4 words (Address bits are A1, A0) no carry from A1 to A2 8 words (Address bits are A2, A1, A0) no carry from A2 to A3
Data 1	n + 1	
Data 2	n + 2	
Data 3	n + 3	
Data 4	n + 4	
Data 5	n + 5	
Data 6	n + 6	
Data 7	n + 7	

- Addressing sequence for Sequential mode

  A column access is performed by incrementing the column address input to the device. The Address is varied by the Burst Length as shown in Table 2.

- Addressing sequence for Interleave mode

  A column access is started from the column address that is input and is performed by inverting the address bits in the sequence shown in Table 3.

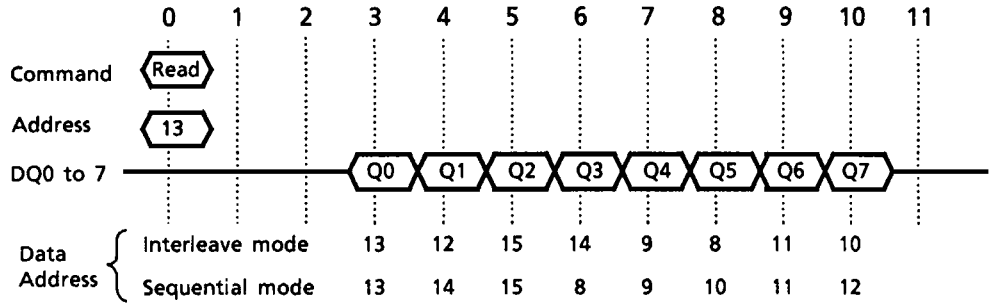
Table 3 Addressing sequence for Interleave mode

Data	Access Address	Burst Length
Data 0	A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words 4 words 8 words
Data 1	A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	
Data 3	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	
Data 4	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0	
Data 5	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$	
Data 6	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0	
Data 7	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$	

Addressing sequence example (Burst Length = 8 and input address is 13)

Data	Interleave mode										Sequential mode		
	A8	A7	A6	A5	A4	A3	A2	A1	A0	Addr		Addr	
Data 0	0	0	0	0	0	1	1	0	1	13	13	13	calculated using A2, A1 and A0 bits. no carry from A2 to A3 bit.
Data 1	0	0	0	0	0	1	1	0	0	12	13 + 1	14	
Data 2	0	0	0	0	0	1	1	1	1	15	13 + 2	15	
Data 3	0	0	0	0	0	1	1	1	0	14	13 + 3	8	
Data 4	0	0	0	0	0	1	0	0	1	9	13 + 4	9	
Data 5	0	0	0	0	0	1	0	0	0	8	13 + 5	10	
Data 6	0	0	0	0	0	1	0	1	1	11	13 + 6	11	
Data 7	0	0	0	0	0	1	0	1	0	10	13 + 7	12	

Read cycle $\overline{CAS}$ latency = 3



- $\overline{CAS}$ Latency field (A6 to A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first data read. The minimum values of $\overline{CAS}$ Latency depend on the frequency of CLK. The minimum value which satisfies the following formula must be set in this field.

t_{CAC} (min) $\leqq$ $\overline{CAS}$ Latency $\times$ t_{CK}

A6	A5	A4	$\overline{CAS}$ Latency
0	0	1	1 clock
0	1	0	2 clock
0	1	1	3 clock

- Test mode entry bit (A7)

This bit is used to enter Test mode and must be set to "0" for normal operation.

- Reserved bits (A8, A10, BS)

These bits are reserved for future operations. They must be set to "0" for normal operation.

- Single Write mode (A9)

This bit is used to select the write mode. When the A9 bit is "0", Burst Read and Burst Write mode are selected. When the A9 bit is "1", Burst Read and Single Write mode are selected.

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

8. Refresh operation

Two types of Refresh operation can be performed on the device: Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$-before-$\overline{RAS}$ refresh of conventional DRAMs and is performed by issuing the Auto Refresh command while both banks are in the idle state. By repeating the Auto Refresh cycle, each bank in turn is refreshed automatically. The Refresh operation must be performed 4096 times (rows) within 64ms (Figure 11). The period between the Auto Refresh command and the next command is specified by t_{RC}.

Self Refresh mode is entered by issuing the Self Refresh command (CKE asserted "low") while both banks are in the idle state. The device is in Self Refresh mode for as long as CKE is held "low". In Self Refresh mode all input/output buffers (except the CKE buffer) are disabled, resulting in lower power dissipation (Figure 13).

9. Power Down Mode

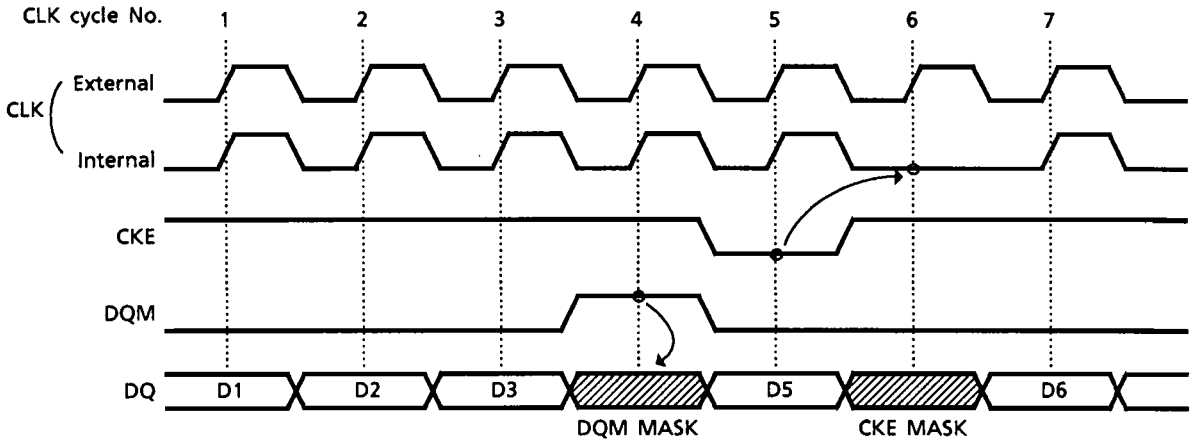
When the device enters Power Down mode, all input/output buffers (except the CKE buffer) are disabled resulting in lower power dissipation in the idle state. Power Down mode is entered by asserting CKE "low" while the device is not running a Burst cycle. Taking CKE "high" exits this mode. When CKE goes high, a No-Operation command must be input at the next rising edge of CLK (Figure 13).

10. CLK suspension and Input / Output Mask

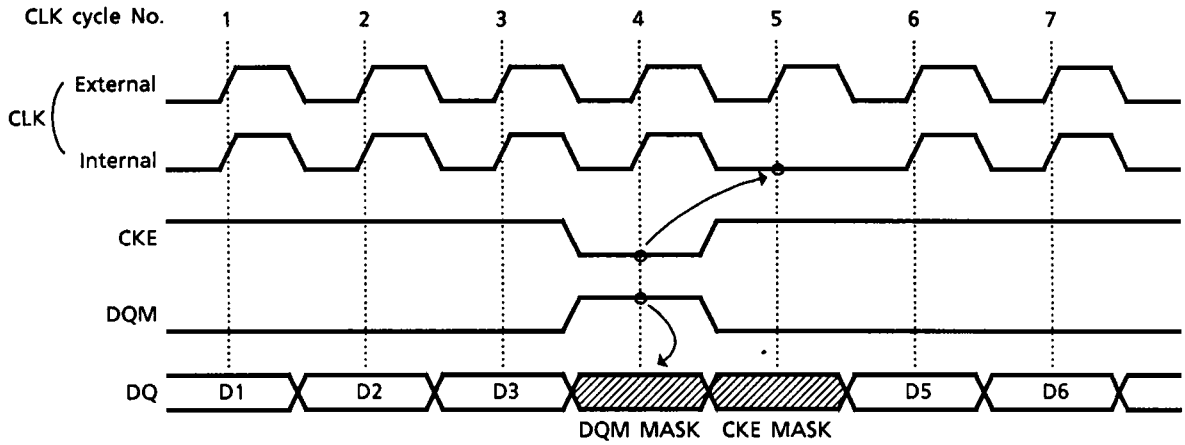
When the device is running a Burst cycle, the internal CLK is suspended by asserting CKE "low" and is frozen from the next cycle. A Read/Write operation is held intact until the CKE signal is taken "high".

The Output Disable/Write Mask signal (DQM) has two functions: controlling the output data in a Read cycle and performing word mask in a Write cycle. When DQM is asserted "high" at the positive edge of CLK, the output data is disabled after two clock cycles in the case of a Read operation; the output data is masked on the same clock cycle in the case of a Write operation. The relation between the CKE timing and DQM is described in Figures 14(a) and 14(b).

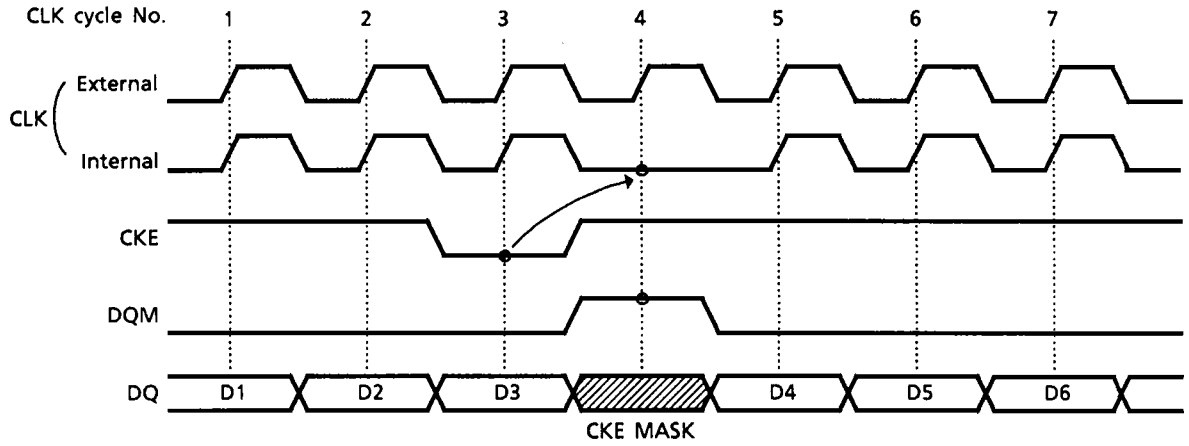
Figure14 (a). CKE/DQM Input timing (Write cycle)



(1)

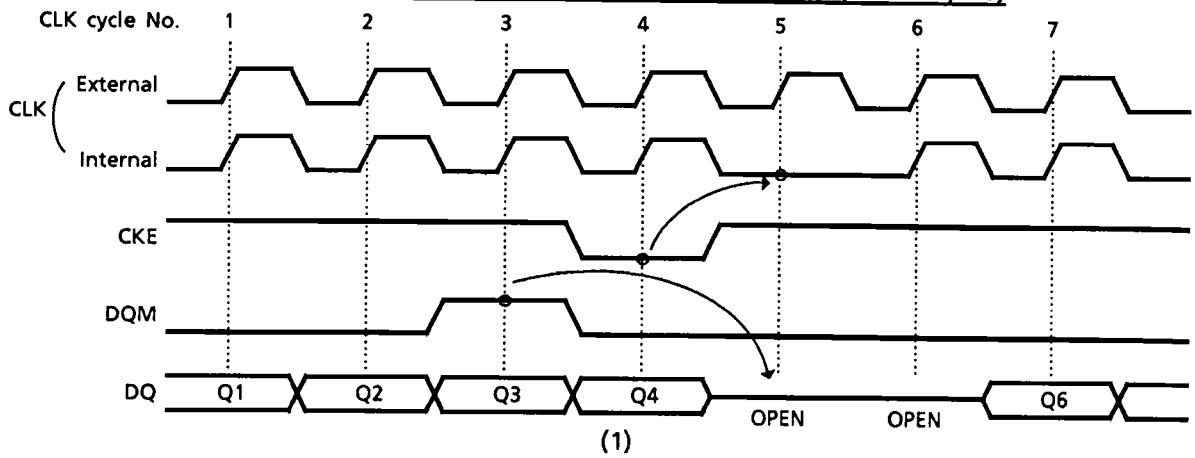


(2)

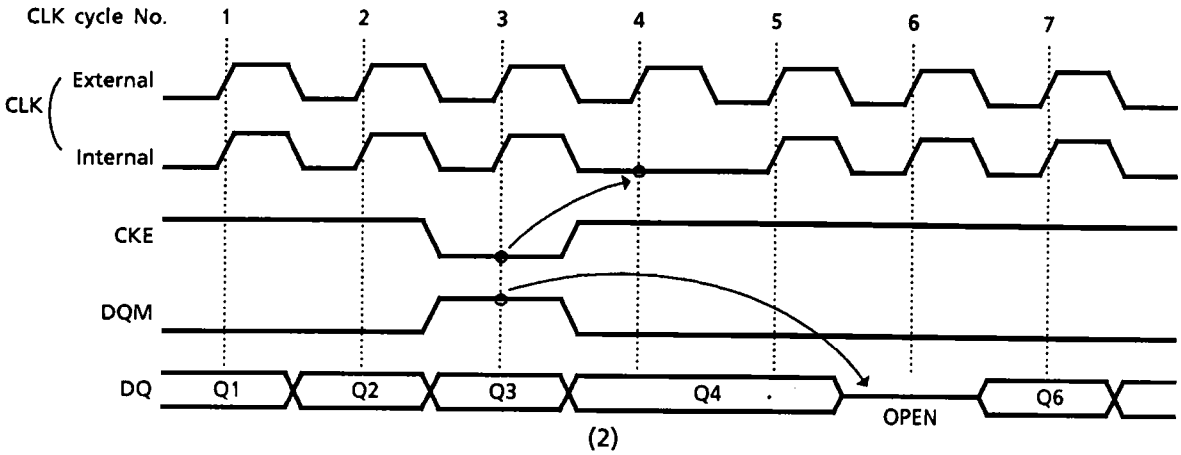


(3)

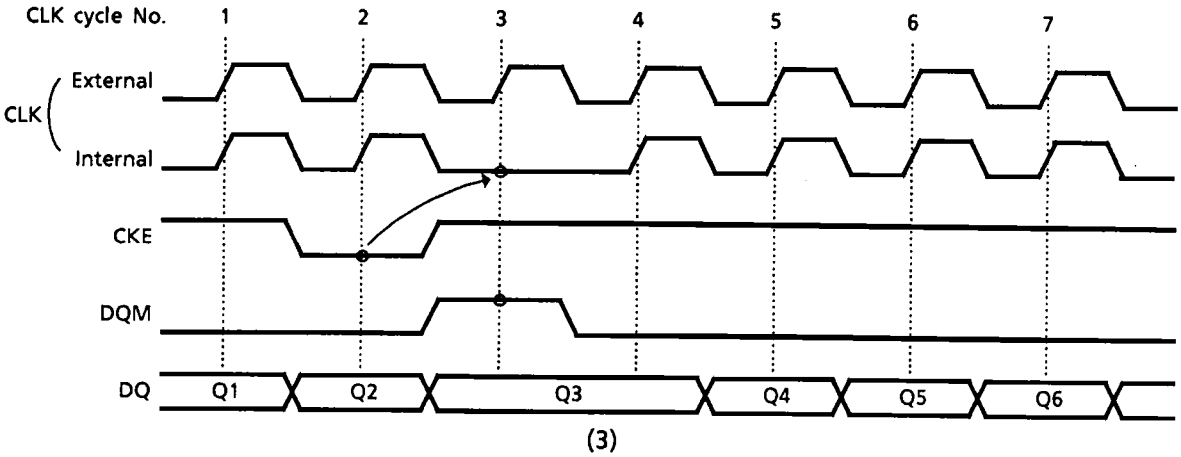
Figure14 (b). CKE, DQM input timing (Read cycle)



(1)

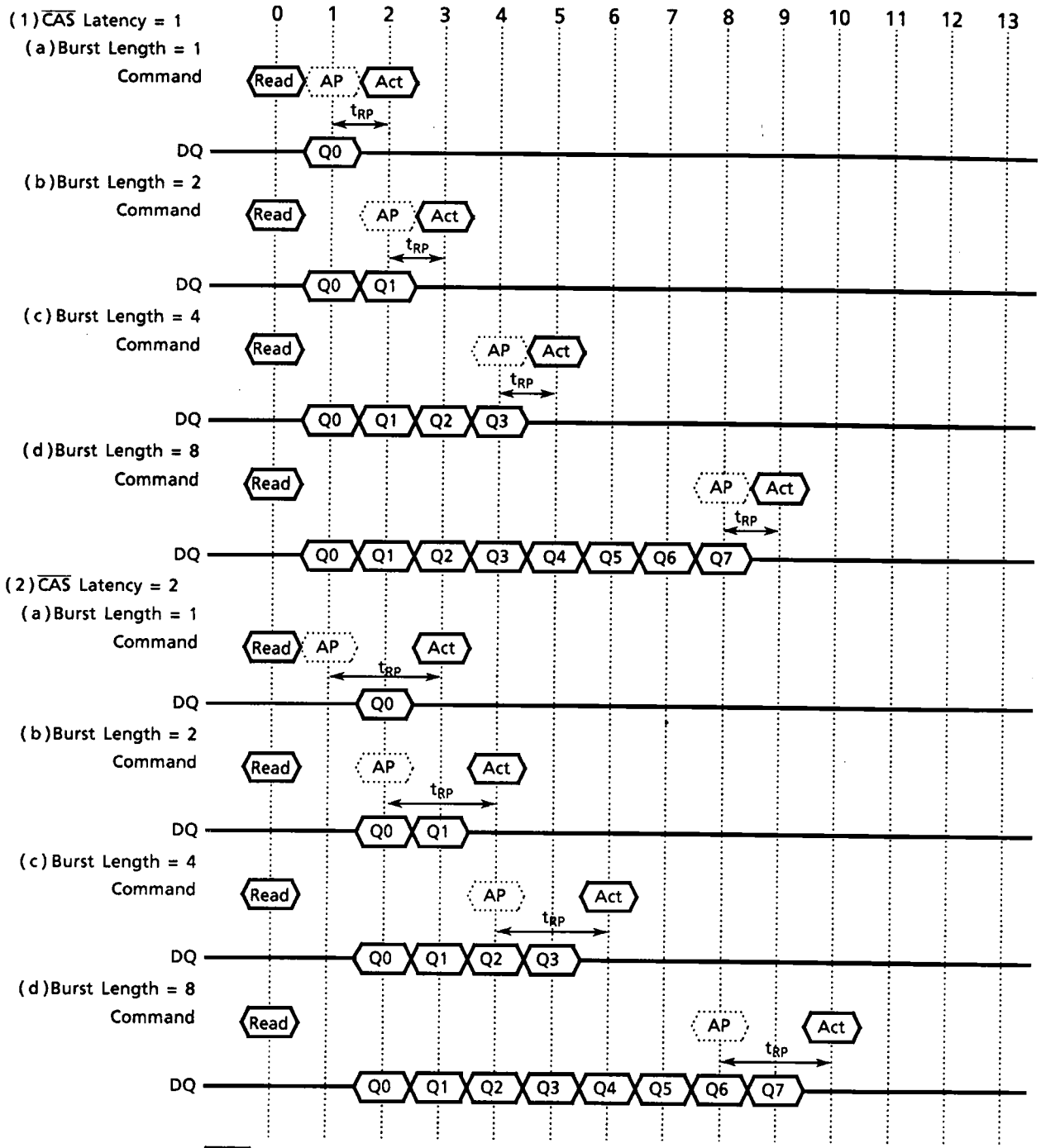


(2)



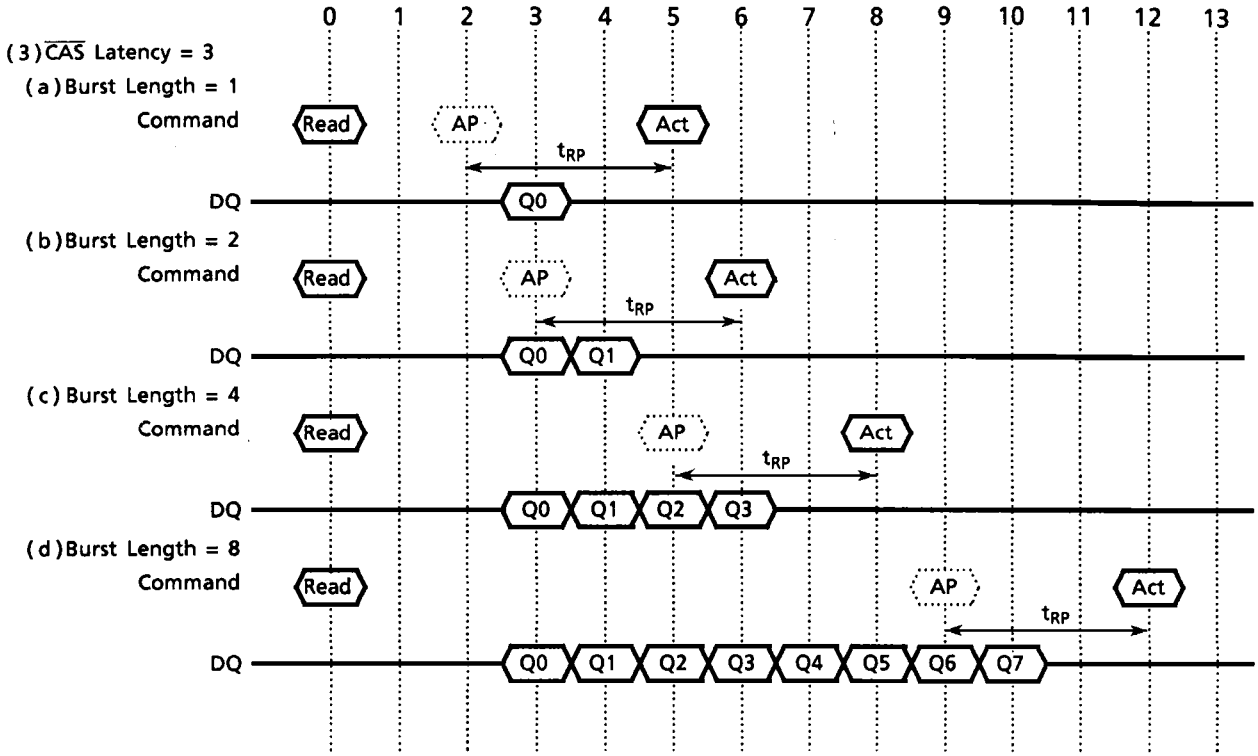
(3)

Figure15 - 1 Auto Precharge timing (Read Cycle)



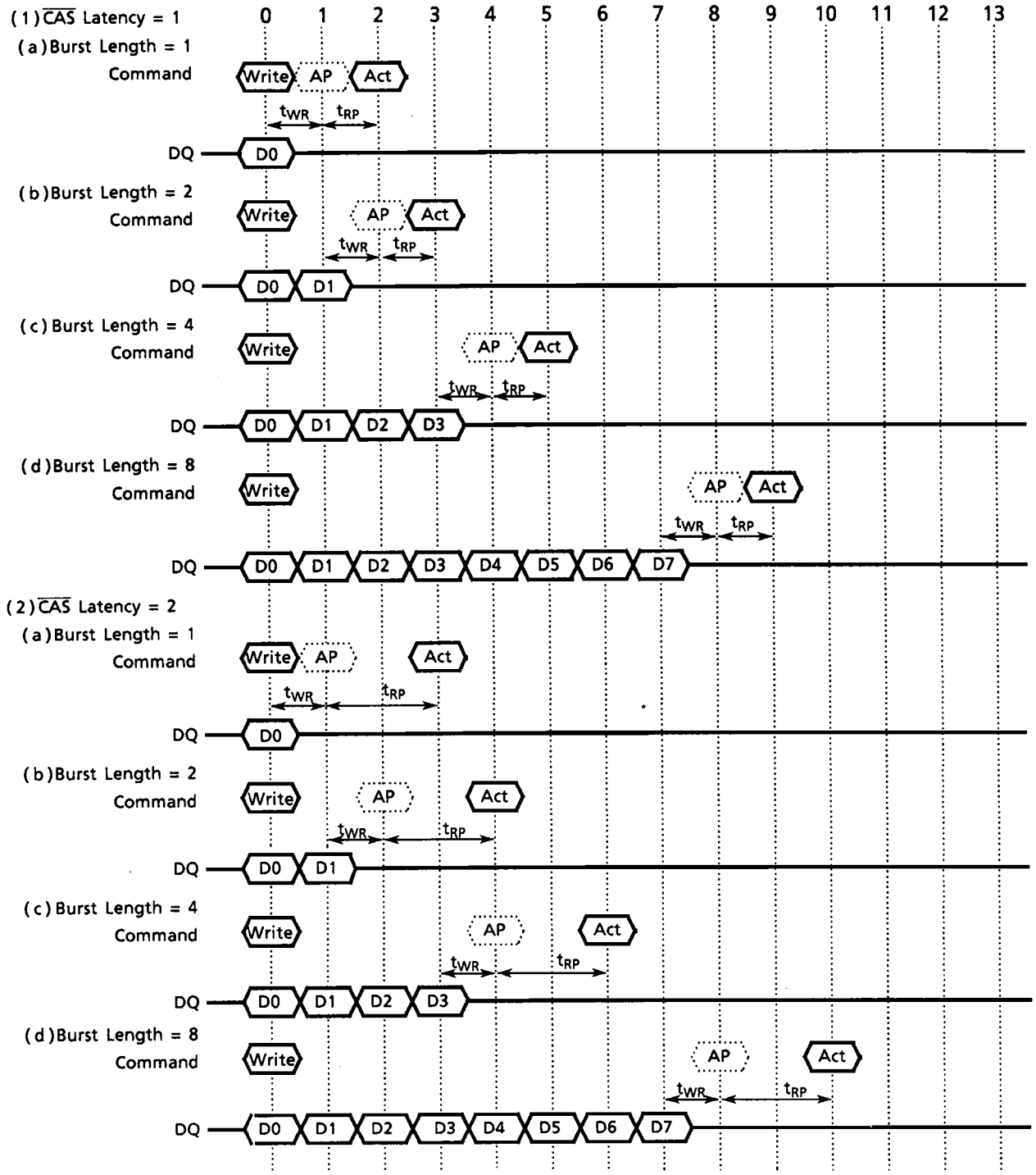
NOTE)
- Read represents the Read with Auto Precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Activate command.
- When the Auto Precharge command is asserted, the period from Bank Activate command to the start of internal precharging must be at least t_{RAS} (min).

Figure15 - 2 Auto Precharge timing (Read Cycle)



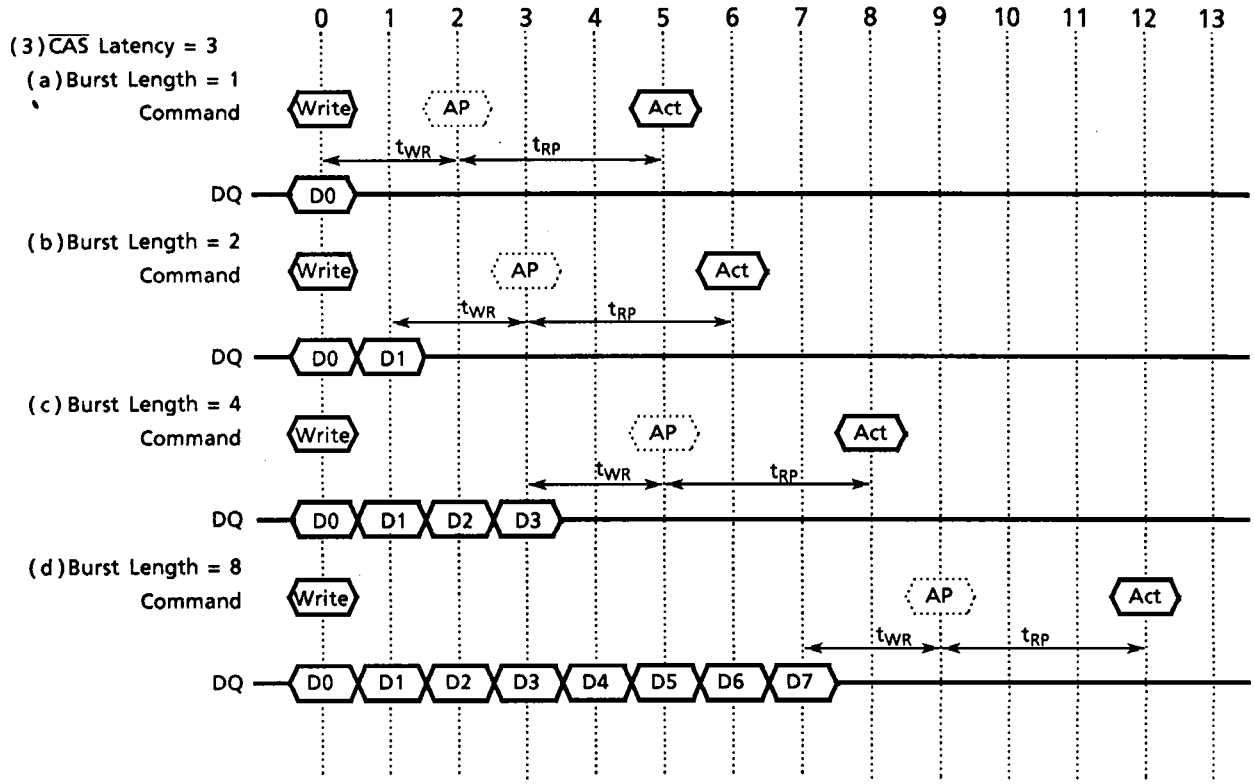
NOTE)
- Read represents the Read with Auto Precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Activate command.
- When the Auto Precharge command is asserted, the period from Bank Activate command to the start of internal precharging must be at least t_{RAS} (min).

Figure16 - 1. Auto Precharge timing (Write Cycle)



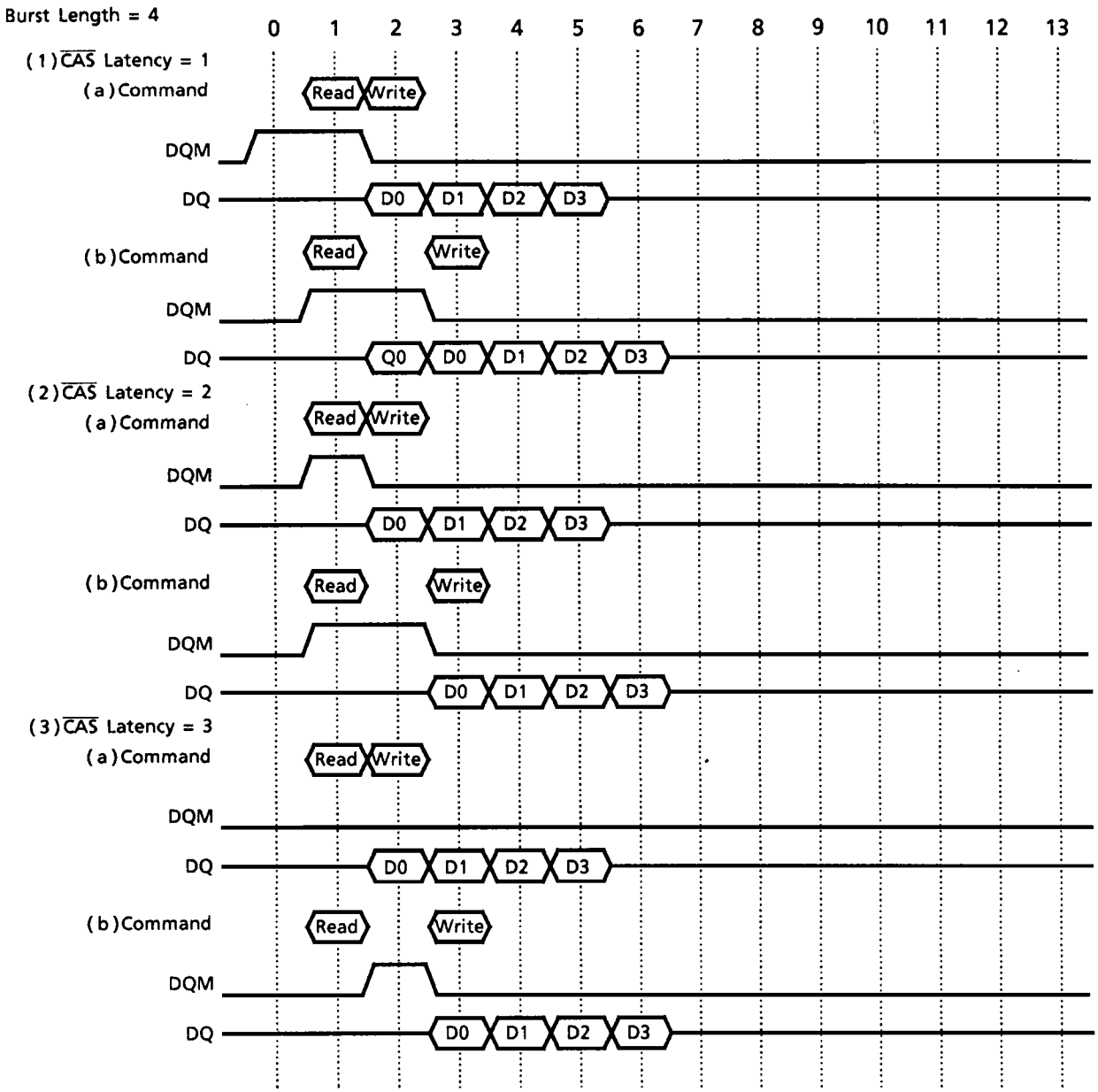
NOTE)
- Read represents the Read with Auto Precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Activate command.
- When the Auto Precharge command is asserted, the period from Bank Activate command to the start of internal precharging must be at least t_{RAS} (min).

Figure16 - 2. Auto Precharge timing (Write Cycle)



NOTE)
- Read represents the Read with Auto Precharge command.
- AP represents the start of internal precharging.
- Act represents the Bank Activate command.
- When the Auto Precharge command is asserted, the period from Bank Activate command to the start of internal precharging must be at least t_{RAS} (min).

Figure 17. Timing chart for Read-to-Write cycle



NOTE) • The output data must be masked by DQM to avoid I/O conflict.

Figure 18. Timing chart of Write-to-Read cycle

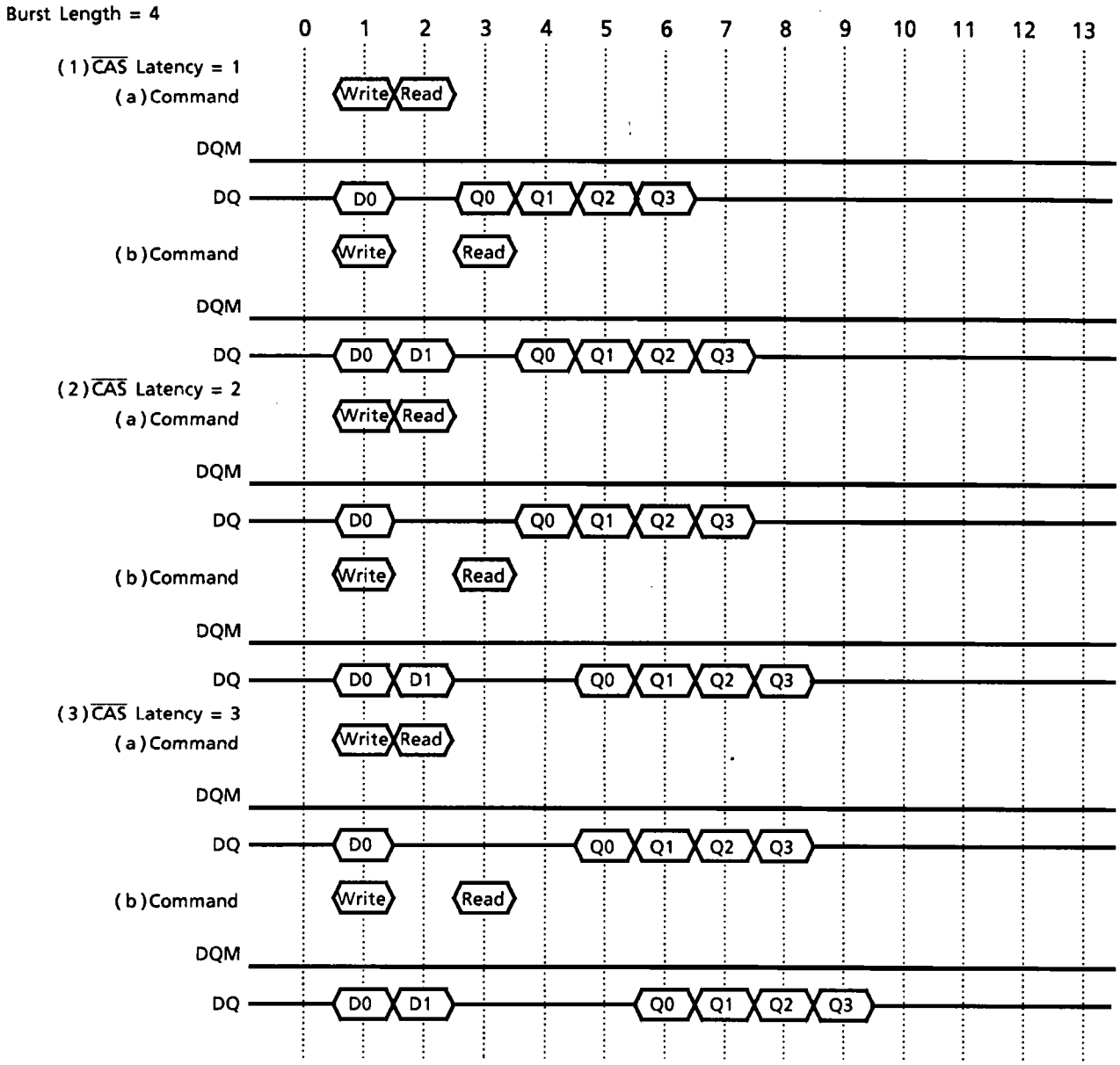
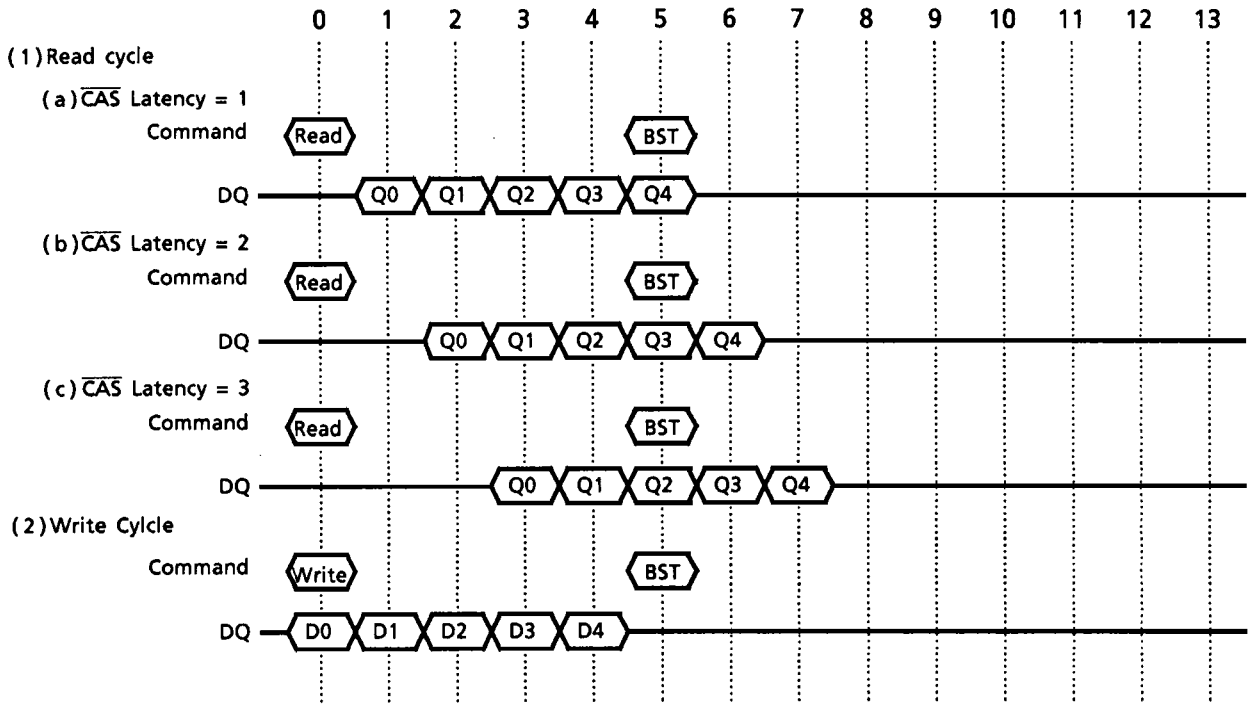
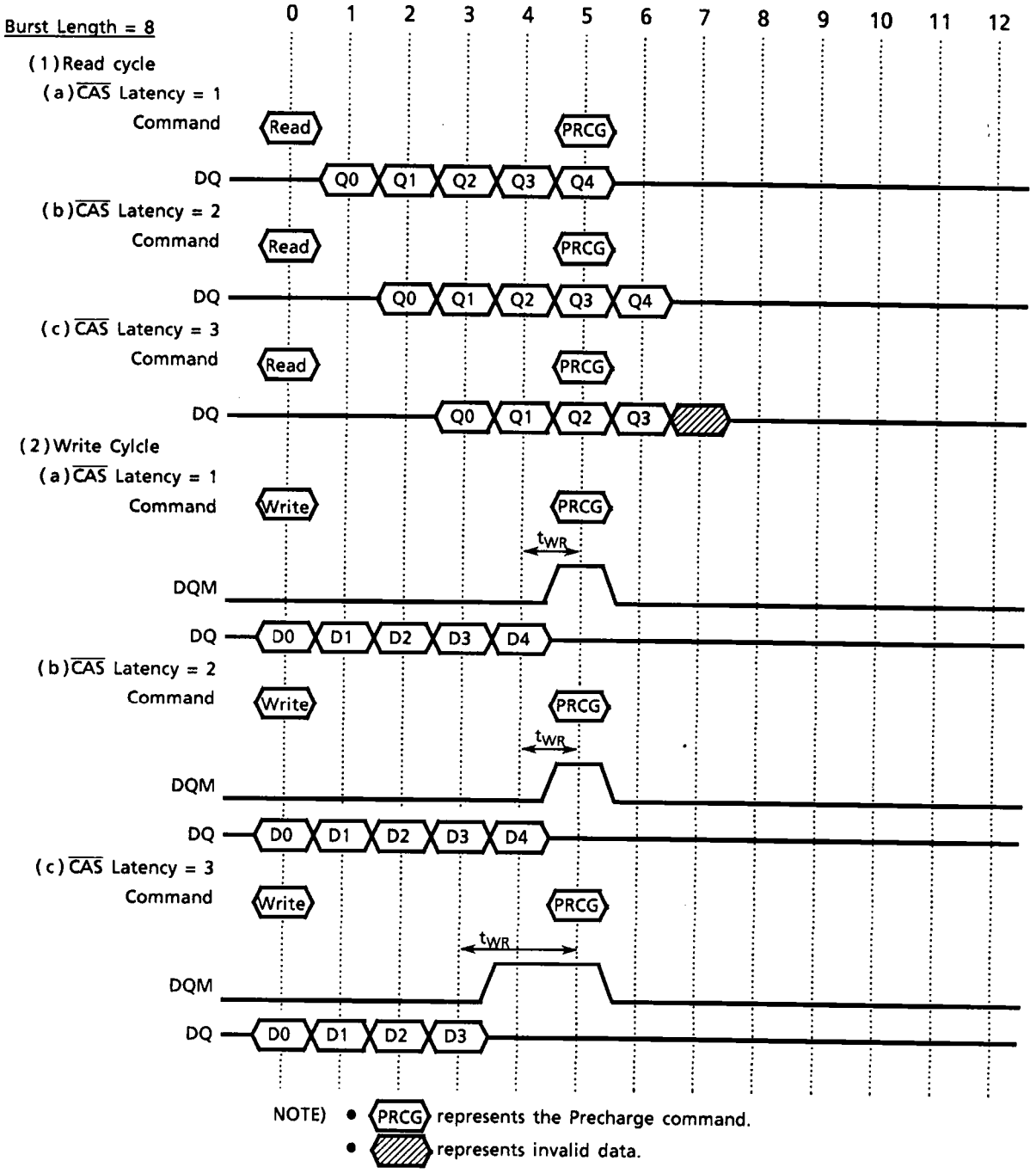


Figure 19. Timing chart of Burst Stop cycle (Burst stop command)



NOTE) • BST represents the Burst stop command.
• The Burst stop command is effective in a Full-page cycle.

Figure 20. Timing chart of Burst Stop cycle (Precharge command)



NOTE) • PRCG represents the Precharge command.
• represents invalid data.

PACKAGE DIMENSIONS (TSOPII 50 - P - 400 - 0.80B)

Units in mm