Signetics

PLS153
Field-Programmable Logic Array (18 × 42 × 10)

Signetics Programmable Logic
Product Specification

Application Specific Products
- **Series 20**

DESCRIPTION

The PLS153 is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS153 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes are contained on the pages following.

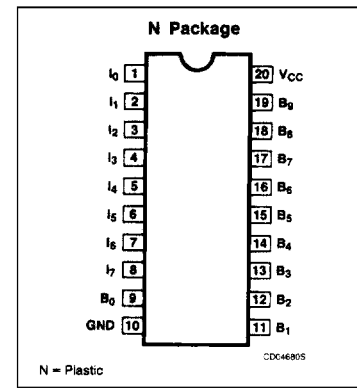
FEATURES

- **Field-Programmable (Ni-Cr links)**
- **8 inputs**
- **42 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active-High or -Low outputs**
- **42 product terms:**
  - **32 logic terms**
  - **10 control terms**
- **I/O propagation delay: 40ns (max.)**
- **Input loading: −100μA (max.)**
- **Power dissipation: 650mW (typ.)**
- **Tri-state outputs**
- **TTL compatible**

APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

PIN CONFIGURATION



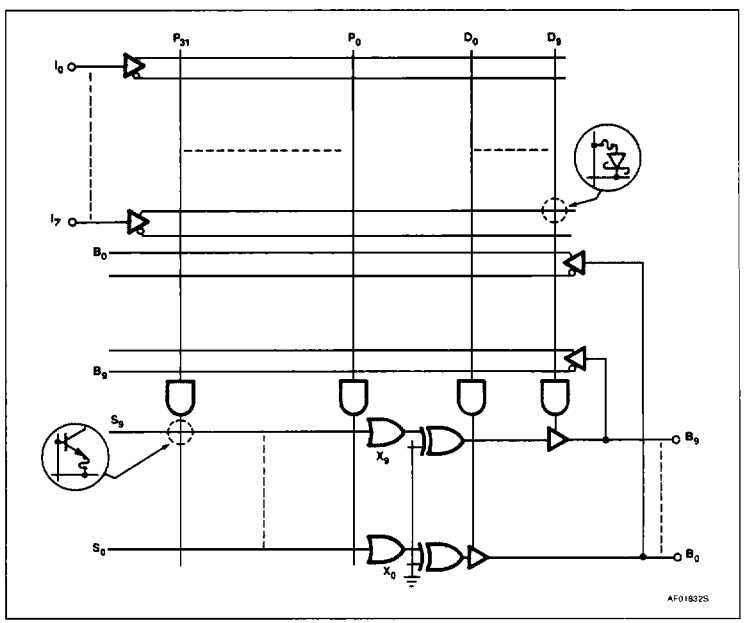
LOGIC FUNCTION

TYPICAL PRODUCT TERM:
$Pn = A \cdot B \cdot C \cdot D \cdot \ldots$
TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L
$\bar{Z} = \overline{P0 + P1 + P2} + \ldots$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:
1. For each of the 10 outputs, either function Z (Active-High) or $\bar{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

FUNCTIONAL DIAGRAM



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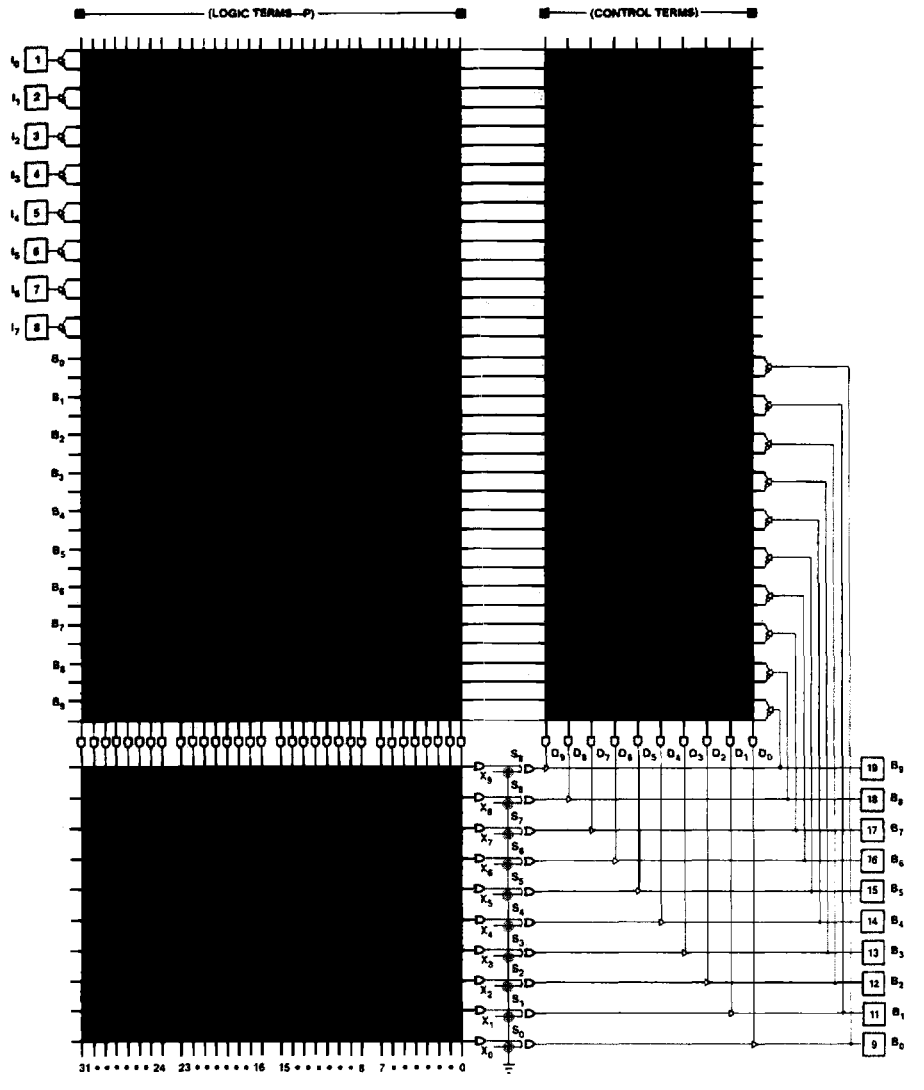
FPLA LOGIC DIAGRAM



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ● [redacted]

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ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Plastic DIP 300mil-wide	PLS153N

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			
T_A	Operating	0	+75	°C
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS153 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

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DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
Input voltage[3]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	
Output voltage						
V_{OL}	Low[3,5]	V_{CC} = Min I_{OL} = 15mA			0.5	V
V_{OH}	High[3,6]	I_{OH} = −2mA	2.4			
Input current[11]						
I_{IL}	Low	V_{CC} = Max V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			40	
Output current						
$I_{O(OFF)}$	Hi-Z state[10]	V_{CC} = Max V_{OUT} = 5.5V			80	μA
		V_{OUT} = 0.45V			−140	
I_{OS}	Short circuit[4,6,7]	V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		130	155	mA
Capacitance						
C_{IN}	Input	V_{CC} = 5V V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		

Notes on following page.

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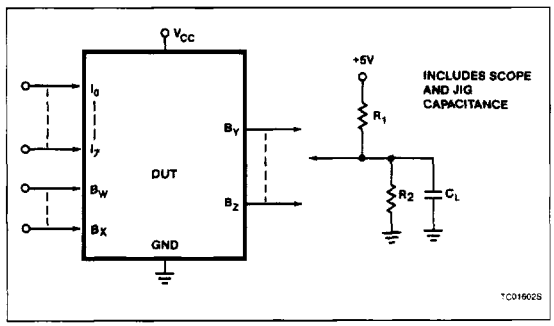
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

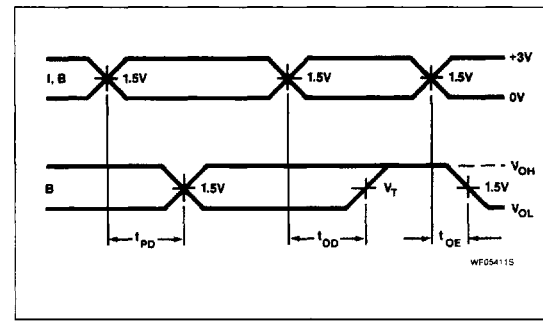
SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ[2]	Max	
t_{PD}	Propagation delay	Output±	Input±	$C_L = 30pF$		30	40	ns
t_{OE}	Output enable	Output–	Input±	$C_L = 30pF$		25	35	ns
t_{OD}	Output disable[9]	Output+	Input±	$C_L = 5pF$		25	35	ns

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with +10V applied to I_7.
6. Measured with +10V applied to I_{0-7}. Output sink current is supplied through a resistor to V_{CC}.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with I_0, I_1 at 0V, $I_2 - I_7$ and B_{0-9} at 4.5V.
9. Measured at $V_T = V_{OL} + 0.5V$.
10. Leakage values are a combination of input and output leakage.
11. I_{IL} and I_{IH} limits are for dedicated inputs only (I_0-I_7).

TEST LOAD CIRCUIT



TIMING DIAGRAM



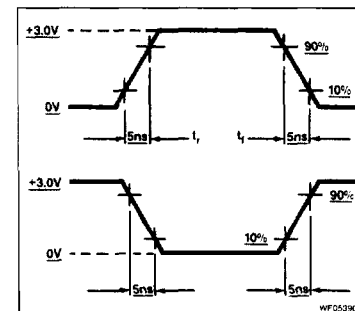
TIMING DEFINITIONS

t_{PD} Propagation delay between input and output.

t_{OD} Delay between input change and when output is off (Hi-Z or High).

t_{OE} Delay between input change and when output reflects specified output level.

VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

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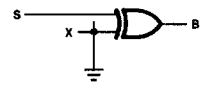
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

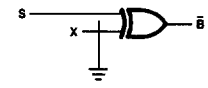
With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this Table the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding links defined as follows:

OUTPUT POLARITY – (B)

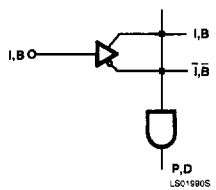


ACTIVE LEVEL	CODE
HIGH[1]	H

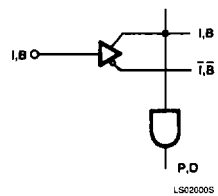


ACTIVE LEVEL	CODE
LOW	L

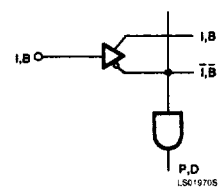
"AND" ARRAY – (I, B)



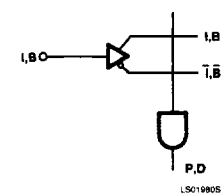
STATE	CODE
INACTIVE[1,2]	O



STATE	CODE
I, B	H

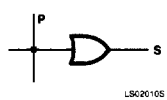


STATE	CODE
Ī, B̄	L

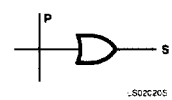


STATE	CODE
DON'T CARE	-

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A



P_n STATUS	CODE
INACTIVE	•

NOTES:
1. This is the initial unprogrammed state of all links.
2. Any gate P_n will be unconditionally inhibited if both the true and complement of an input (either I or B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

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FPLA PROGRAM TABLE