October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB834200A-20

CMOS 4M–BIT MASK PROGRAMMABLE READ ONLY MEMORY

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4M–BIT (256K x 16, 512K x 8) CMOS READ ONLY MEMORY

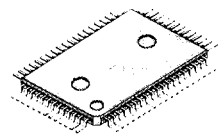
The Fujitsu MB834200A is a CMOS Si–gate mask–programmable static read only memory organized as 262,144 words by 16 bits. (524,288 words by 8 bits).

The MB834200A has TTL–compatible I/O 3–state output level with full–static operation (i.e. no need of clock signal) and single +5V power supply.

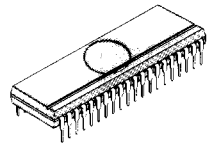
Also, the MB834200A is designed for applications such as character generator or program storage which require large memory capacity and high–speed/low–power operation.

Memory organization of MB834200A is changeable between 16 bits and 8 bits. (ex. The system using 8 bits CPU and 16 bits CPU can use common data on the same chip.)

- Organization: 262,144 words x 16 bits
  524,288 words x 8 bits
- Access time: 200ns max.
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5V power supply
- Power dissipation: 220mW max. (Active)
  5.5mW max. (Standby, TTL Input level)
  275µW max. (Standby, CMOS input level)
- Standard 40–pin Plastic DIP
- 64–pin Plastic Quad Flat Package



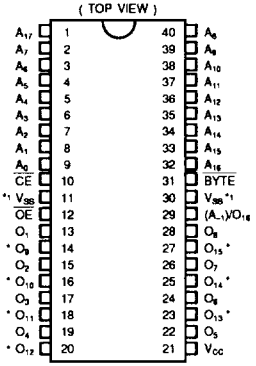
PLASTIC PACKAGE
FPT–64P–M01



PLASTIC PACKAGE
DIP–40P–M01

PIN ASSIGNMENT

(TOP VIEW)



* is applied to 8 bits.
* 1: All connect to V_{SS}.
QFP: See 6page.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to +7.0 *	V
Input Voltage	V_{IN}	–0.5 to V_{CC} +0.5 *	V
Output Voltage	V_{OUT}	–0.5 to V_{CC} +0.5 *	V
Temperature Under Bias	T_{BIAS}	–10 to +85	°C
Storage Temperature Range	T_{STG}	–45 to +125	°C

*** Referenced to GND**

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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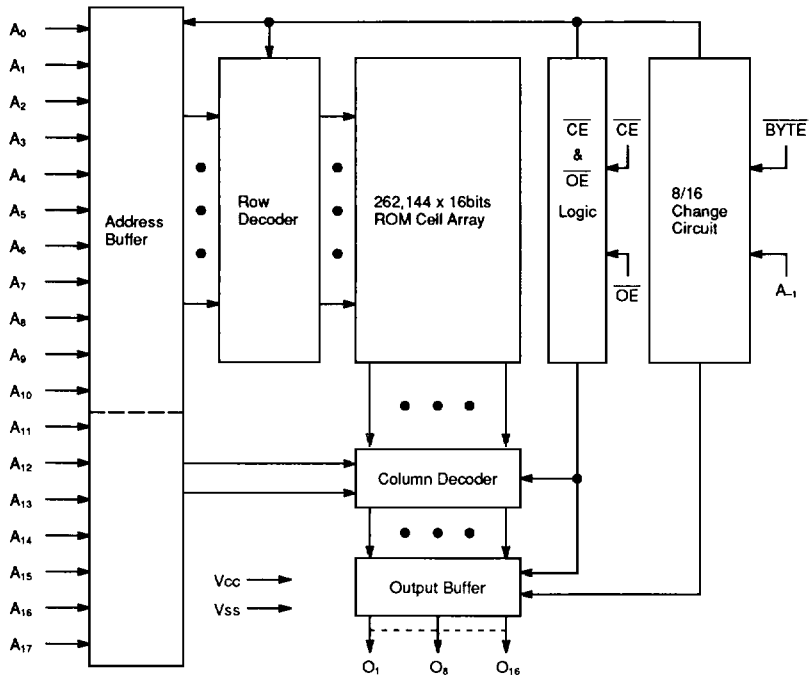
Fig. 1 — MB834200A BLOCK DIAGRAM



OUTPUT SELECTION MODE

A_{-1}	$\overline{BYTE}$	O_1 to O_8	O_9 to O_{15}	O_{16}
X	H	O_1 to O_8	O_9 to O_{15}	O_{16}
L	L	O_1 to O_8	High–Z	A_{-1}
H	L	O_9 to O_{16}	High–Z	A_{-1}

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	Mode	Output	Power Dissipation Mode
H	X	Not Selected	High–Z	Standby
L	H	Not Selected	High–Z	Active
L	L	Selected	D_{OUT}	Active

CAPACITANCE (TA=25° C, f=1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			15	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Ambient Temperature	T_A	0		70	°C

DC CHARACTERISTICS

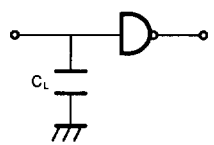
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Active Supply Current	$\overline{CE}$=V_{IL}, Minimum Cycle	I_{CC}			40	mA
Standby Supply Current	$\overline{CE}$=V_{IH}	I_{SB1}			1	mA
	$\overline{CE}$=V_{CC}=V_{IH}, V_{IN}=V_{SS} or V_{CC}	I_{SB2}			50	µA
Input Leakage Current	V_{IN}=0 to V_{CC}	I_{LI}	−10		10	µA
Output Leakage Current	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IH}	I_{LO}	−10		10	µA
Output High Voltage	I_{OH}=−400µA	V_{OH}	2.4			V
Output Low Voltage	I_{OL}=2.1mA	V_{OL}			0.4	V

Fig. 2 — AC TEST CONDITION

- Input Pulse Level : 0.6 to 2.4V
- Input Pulse Rise and Fall Time : t_T=5ns
- Timing Reference Levels : Input: V_{IL}=0.8V, V_{IH}=2.2V
  Output: V_{OL}=0.8V, V_{OH}=2.2V
  : 1 TTL Gate and 100pF

- Output Load



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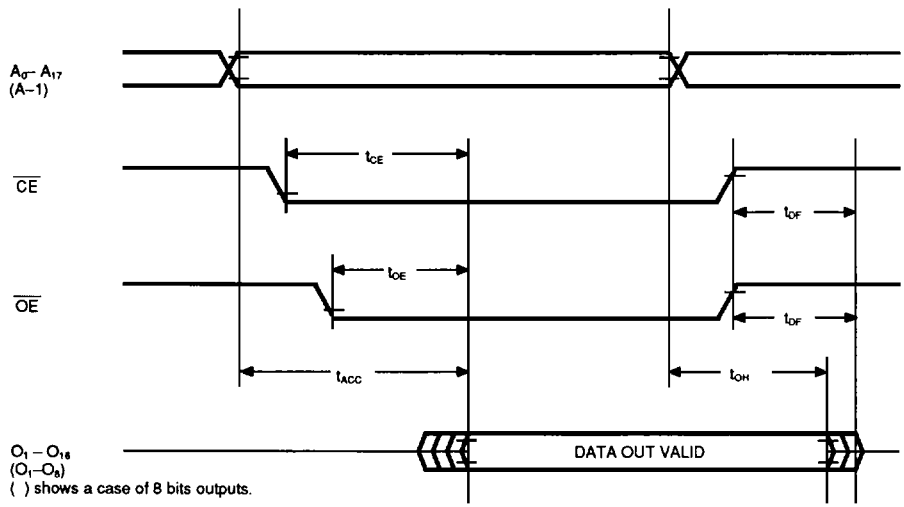
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	t_{ACC}		200	ns
Chip Enable Access Time	$\overline{OE}=V_{IL}$	t_{CE}		200	ns
Output Enable Access Time	* 1	t_{OE}		80	ns
Output Disable Time	* 2	t_{DF}		60	ns
Output Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	t_{OH}	0		ns

* 1: Maximum $\overline{OE}$ delay which does not afftect t_{ACC} is $t_{ACC} - t_{OE}$.
* 2: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to High earlier.

TIMING DIAGRAM

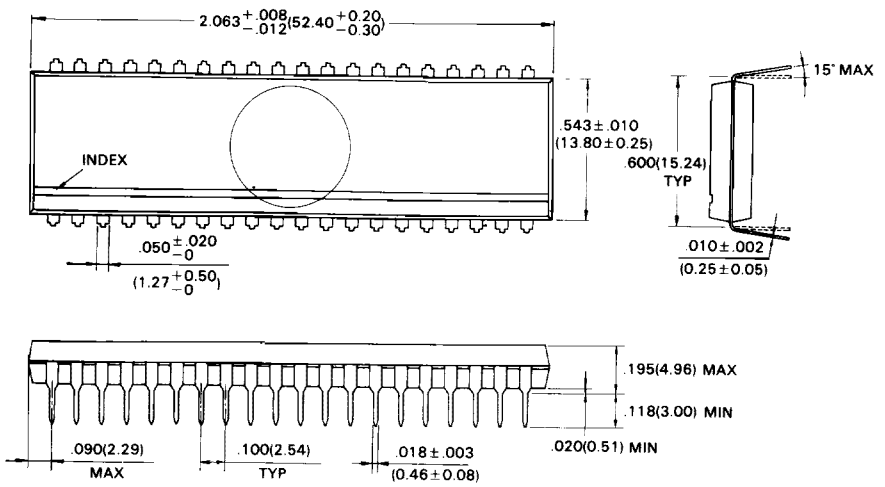


( ) shows a case of 8 bits outputs.

PACKAGE DIMENSIONS

40-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-40P-M01)



Dimensions in inches (millimeters)

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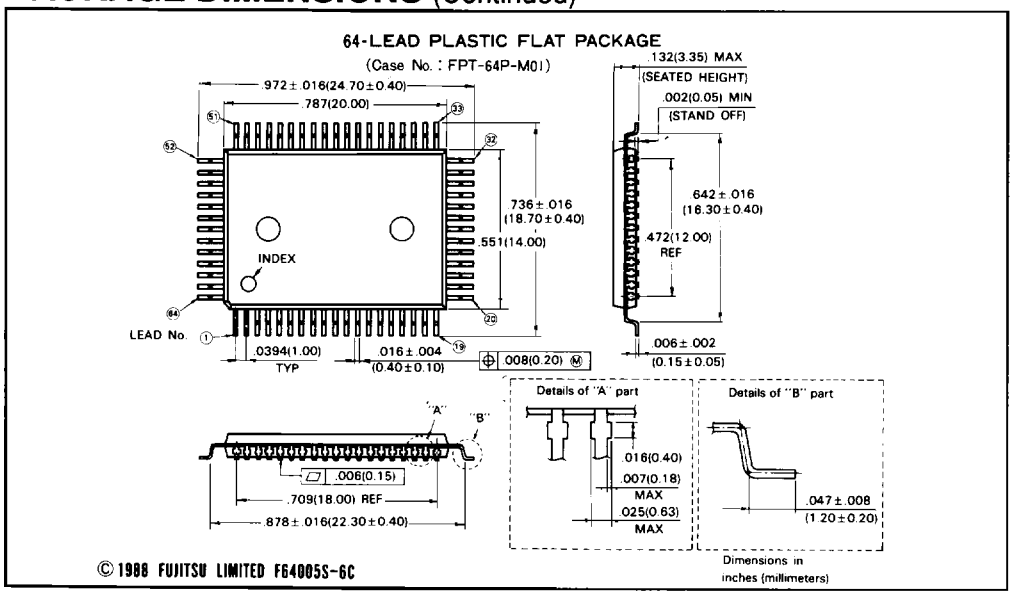
PACKAGE DIMENSIONS (Continued)



PIN ASSIGNMENT